16-channel High Voltage analog switch IC

ECN32910TF/32911TF Product Specification

ECN32910TF/32911TF are 16-channel High Voltage analog switching IC on which latch-up free is realized by SOI isolation technology.

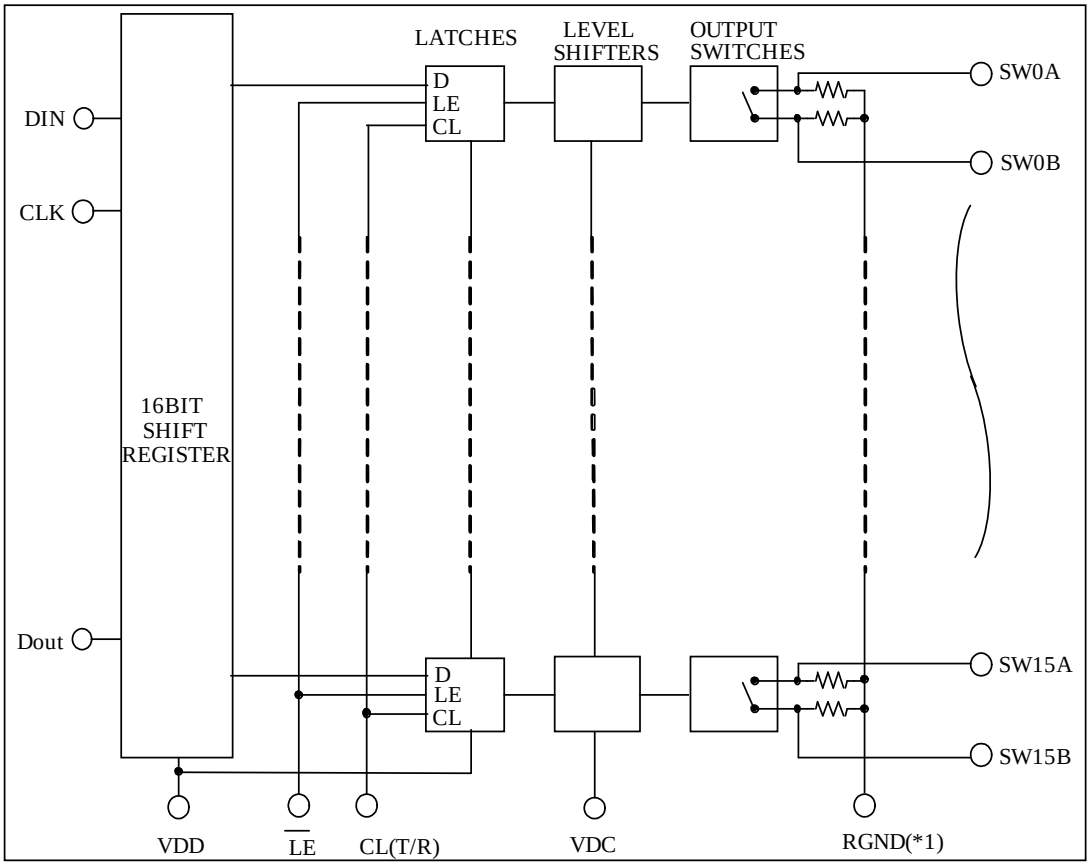
High voltage and low ON-resistance MOS switches are used as output devices controlled by a 3.3V or 5V signal. ECN32910/32911 is the most suited to Ultrasound Imaging applications.

Functions

* High voltage and low on-resistance MOS switches are integrated.
* Integrated 16bit shift resister
* Integrated bleed resistors on the outputs.(ECN32911 only)

Features

* No high voltage power supply required
* Low power consumption
* Switch on-resistance: 18 Ω typ. (ISIG=5mA, 25°C)
* Switch breakdown voltage: 120V
* 48-pin TQFP Package (RoHS compliant)



(*1) ECN32911 integrates bleed resistors which are connected to RGND terminal on i nternal IC

Fig.1 Block diagram

1. General

This Specification shall be applied to the following semiconductor integrated circuit.

1) Parts name : ECN32910TF/32911TF
2) Application : Ultrasound imaging scanner and others
3) Structure : Monolithic IC
4) Package : TQFP48

2. Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Terminal	Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 to +7.0	V	Ta＝25°C
2	VDC voltage supply	VDC	VDC	-0.5 to 15.5	V	Ta＝25°C
3	Logic input voltages	VIN	DIN, CLK, CL, LE	-0.5 to VDD+0.3	V	Ta＝25°C
4	Analog signal range	-	SW0 to SW15	-120 to +120	V	Ta＝25°C
5	Operating junction temperature	Tjop	-	-20 to +125	°C	
6	Storage temperature	Tstg	-	-55 to +150	°C	
7	Power dissipation	Pw	-	1.0	W	TQFP48 Ta＝70°C

3. Electrical Characteristics

3.1 DC Characteristics

Table 2 DC Characteristics Ta=25°C VDC=12V VDD=5V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	Small signal switch on resistance	RONS	–	18	26	Ω	ISIG=5mA
			–	18	26		ISIG=200mA
2	Small signal switch on resistance matching	ΔRONS	–	5	20	%	ISIG=5mA
3	Large signal switch on resistance	RONL	–	16	—	Ω	ISIG=1A
4	Value of output bleed resistance	RINT	20	35	50	kΩ	Output switch to RGND IRINT=0.5mA
5	Switch off leakage per switch	ISOL	–	1	10	μA	VSIG=100V
			–	1(3)	3(7)	mA	VSIG=-100V, 32911 is Enclosed in parenthesis
6	Switch cut off current	ISCC	–	1	10	μA	VSIG=100V or -100V
7	DC offset switch (off)	DCOFF	–	10	100	mV	No load
8	DC offset switch (on)	DCON	–	10	100	mV	No load
9	VDC average current	IDC	–	–	3	mA	fsw=50kHz, No load
10	VDC quiescent current	IDCQ1	–	10	50	μA	All SWs off
		IDCQ2	–	10	50	μA	All SWs on, ISIG=5mA
11	VDC peak current	IDSC	–	–	7	mA	All SWs on, no load, Vsig = -100V
12	VDD average current	IDD	–	–	3.0	mA	fCLK=5MHz,VDD=5.0V
13	VDD quiescent current	IDDQ	–	–	10	μA	
14	Data out source current	ISOR	0.45	0.70	–	mA	VOUT=VDD-0.7V
15	Data out sink current	ISINK	0.45	0.70	–	mA	VOUT=0.7V

3.2 AC Characteristics

Table 3 AC Characteristics Ta=25°C VDC=12V VDD=5V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	SW Turn on time	tON	–	–	3.0	μs	VSIG=100V, RL=10kΩ
2	SW Turn off time	tOFF	–	–	3.0	μs	VSIG=100V, RL=10kΩ
3	Clock frequency	fCLK	–	–	30	MHz	50% duty cycle, fData=fCLK/2 VDD= 5.0V
			–	–	20	MHz	50% duty cycle, fData=fCLK/2 VDD=3.3V
4	Clock delay time to data out	tDO	–	–	48	ns	DOUT terminal,VDD=3.3V
			–	–	32	ns	DOUT terminal,VDD=5.0V

Table 4 AC Characteristics (for reference purpose only) Ta=25°C VDC=12V VDD=5V

No.	Items	Symbol	Spec			Unit	Condition
			Min	Typ	Max		
1	Off capacitance SW to GND	CSG (off)	–	15	–	pF	0V, 1MHz
2	On Capacitance SW to GND	CSG (on)	–	25	–	pF	0V, 1MHz
3	SW off isolation	KO	-28	-32	–	dB	f=5MHz, 1kΩ//15pF load
			-50	-54	–	dB	f=5MHz, 50Ω load
4	SW Crosstalk	KCR	-50	-54	–	dB	f=5MHz, 50Ω load
5	Output voltage spike	+VSPK	–	–	40	mV	RL=50Ω
		-VSPK	-20	–	–		

4. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 5.

Table 5 Recommended Operating Conditions

No	Items	Symbol	Recommended Value	Condition
1	Logic power supply voltage	VDD	3.0V to 5.5V	
2	VDC voltage supply	VDC	10V to 15V	
3	High-level input voltage	VIH	0.9VDD to VDD	
4	Low-level input voltage	VIL	0V to 0.1VDD	
5	Analog signal voltage peak to peak	VSIG	-100V to 100V	
6	Analog signal frequency	Fsig	Min.100KHz	VSIG > 10Vp-p
			Not limited	VSIG ≤ 10Vp-p
7	Operating free air-temperature	Ta	0^{o}C to 70^{o}C	
8	Switching frequency	Fsw	50kHz max, Duty Cycle=50%	
9	Set up time for LE	TSD	Min.60ns	
10	Pulse width of LE	TWLE	Min.40ns	
11	Time width of CL	TWCL	Min.40ns	
12	Set up time DATA to Clock	TSU	Min.10ns	
13	Hold time DATA from Clock	Th	Min.10ns	
14	Maximum VSIG Slew Rate	dV/dt	Max.30V/ns	

Attention ;

1) GND terminal must be connected during power-up and power-down.
2) It is indispensable overshoot/undershoot voltage of power supplies(VDD, VDC) do NOT exceed maximum rated voltage in the event of power-up and power-down.

5. Test Circuit

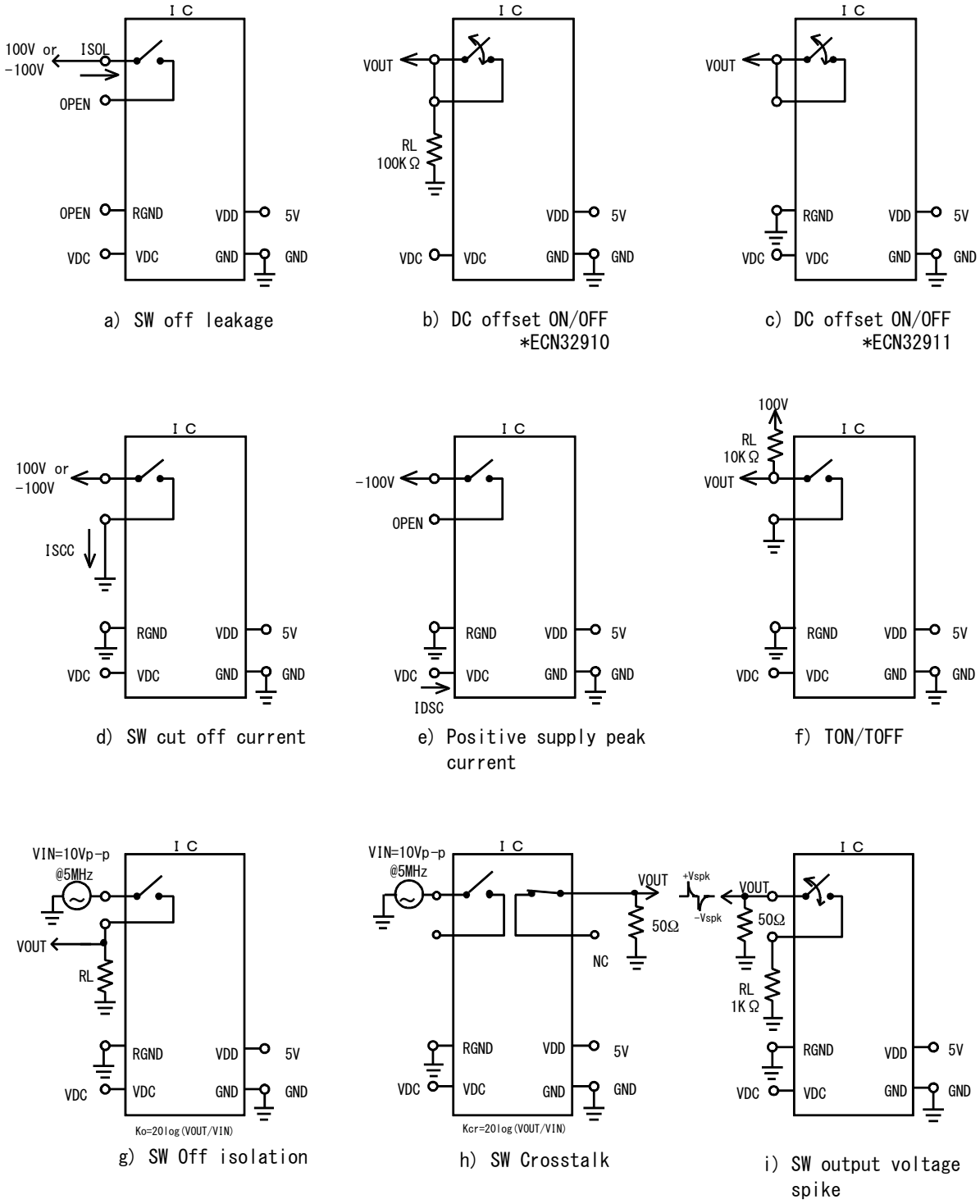


Fig. 2 Test Circuit

6. Timing Waveforms

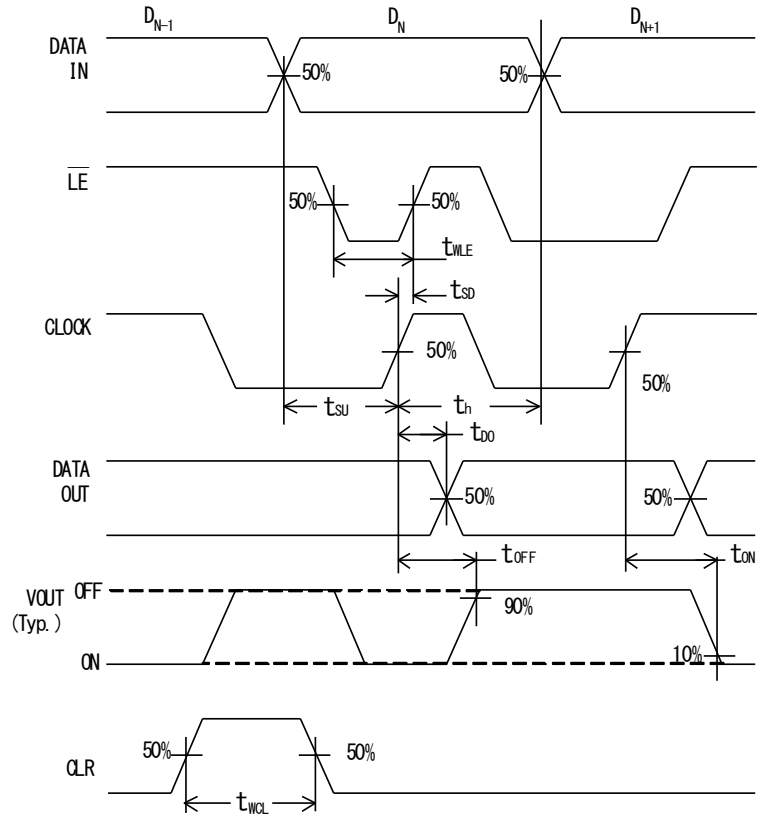


Fig. 3 Timing Waveforms

Note

1. Serial data is clocked in on the rising edge of CLK.

2. The switches go to a state retaining their present condition on the rising edge of LE.

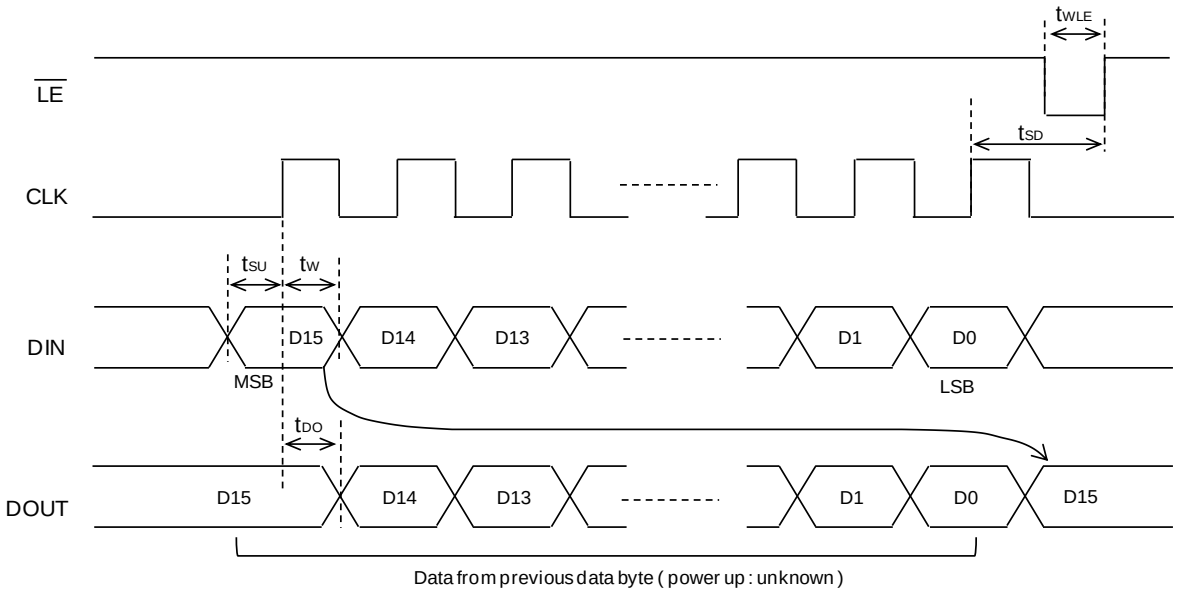


Fig. 4 LATCH ENABLE Timing waveform

7. Truth Table

Table 6 Truth table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

D8	D9	D10	D11	D12	D13	D14	D15	LE	CL	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't care

Note

1. The 16 Switches operate independently.
2. When LE is low, the shift register data flows through the latch.
3. Shift register clocking has no effect on the switch states if LE is high.
4. When switch 15 is ON, DOUT will be high.
5. The clear input overrides all other inputs.

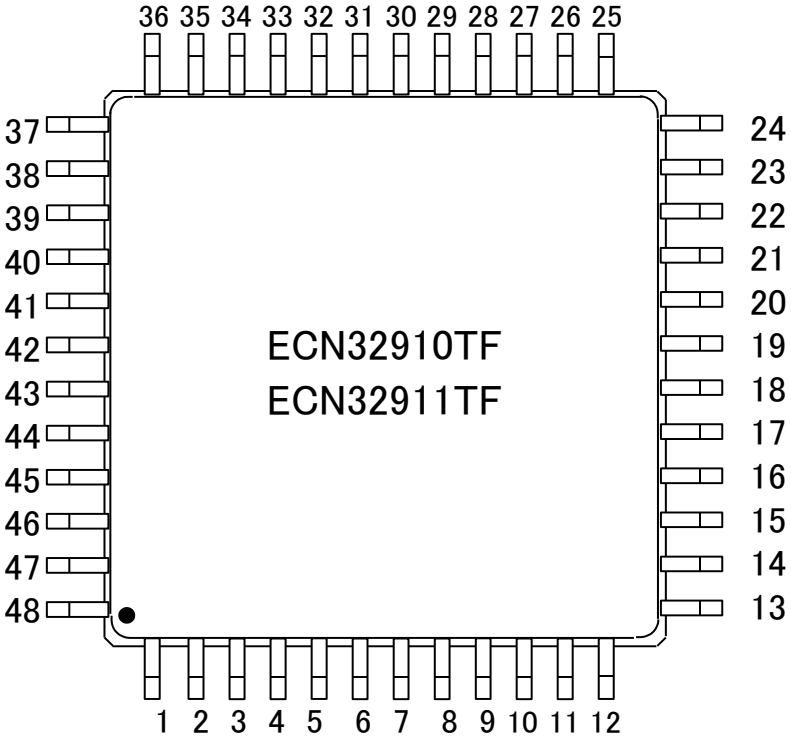
8. Pin Configuration

ECN32910TF/32911TF TQFP48（48Pin TQFP）

Table7. Pin Configuration

Pin	Name	Functions	Note
1	N/C	No connection	*1
2	N/C	No connection	*1
3	SW4B	Analog Switch 4	
4	SW4A	Analog Switch 4	
5	SW3B	Analog Switch 3	
6	SW3A	Analog Switch 3	
7	SW2B	Analog Switch 2	
8	SW2A	Analog Switch 2	
9	SW1B	Analog Switch 1	
10	SW1A	Analog Switch 1	
11	SW0B	Analog Switch 0	
12	SW0A	Analog Switch 0	
13	GND2	Ground	
14	N/C	No connection	*1
15	VDC	VDC voltage supply	
16	N/C	No connection	*1
17	GND	Ground	
18	VDD	Logic Supply Voltage	
19	DIN	Serial Data Input	
20	CLK	Serial Clock Input	
21	$\overline{LE}$	Latch-Enable Input	
22	CLR	Latch-Clear Input	
23	DOUT	Serial Data Output	
24	RGND(N/C)	Ground(ECN32911TF) / No connection(ECN32910TF)	*2
25	SW15B	Analog Switch 15	
26	SW15A	Analog Switch 15	
27	SW14B	Analog Switch 14	
28	SW14A	Analog Switch 14	
29	SW13B	Analog Switch 13	
30	SW13A	Analog Switch 13	
31	SW12B	Analog Switch 12	
32	SW12A	Analog Switch 12	
33	SW11B	Analog Switch 11	
34	SW11A	Analog Switch 11	
35	N/C	No connection	*1
36	N/C	No connection	*1
37	SW10B	Analog Switch 10	
38	SW10A	Analog Switch 10	
39	SW9B	Analog Switch 9	
40	SW9A	Analog Switch 9	
41	SW8B	Analog Switch 8	
42	SW8A	Analog Switch 8	
43	SW7B	Analog Switch 7	
44	SW7A	Analog Switch 7	
45	SW6B	Analog Switch 6	
46	SW6A	Analog Switch 6	
47	SW5B	Analog Switch 5	
48	SW5A	Analog Switch 5	

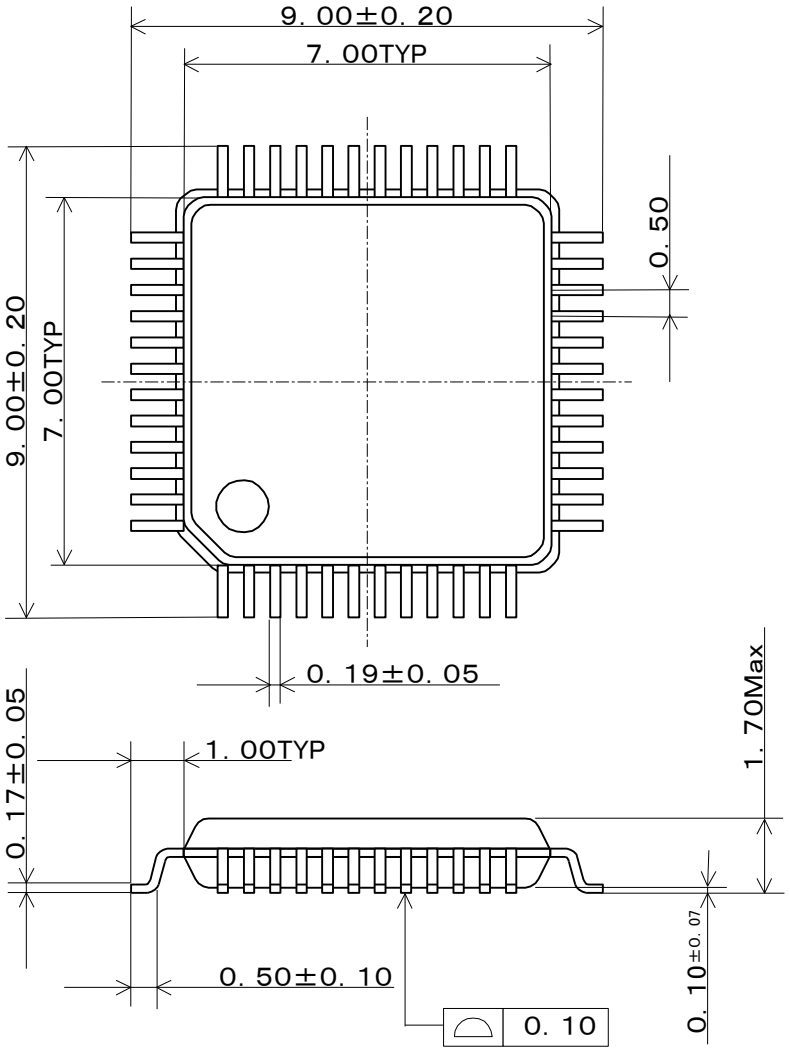
Note 1. NOT connected on chip internal.
2. RGND terminal connects to bleed resistors on chip internal.(ECN32911TF only).



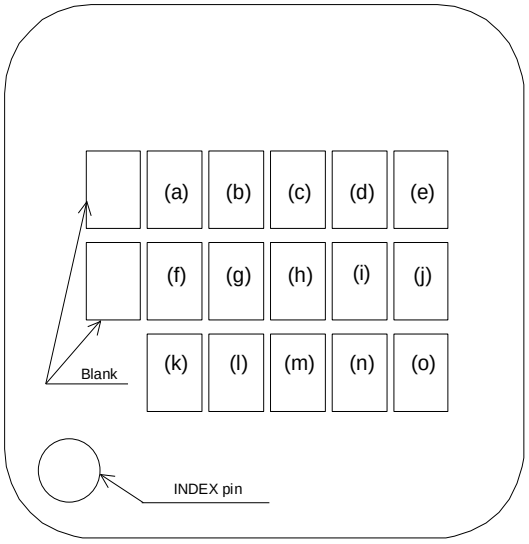
48pin Package

9. Package Outline

Units : mm



10. Marking spec



Lot numbering rule

(a) :Year code (Least significant digit of Assembled year (A.D.))

(b) :Month code (Refer to following table.)

Month	1	2	3	4	5	6	7	8	9	10	11	12
Month code	A	B	C	D	E	K	L	M	N	X	Y	Z

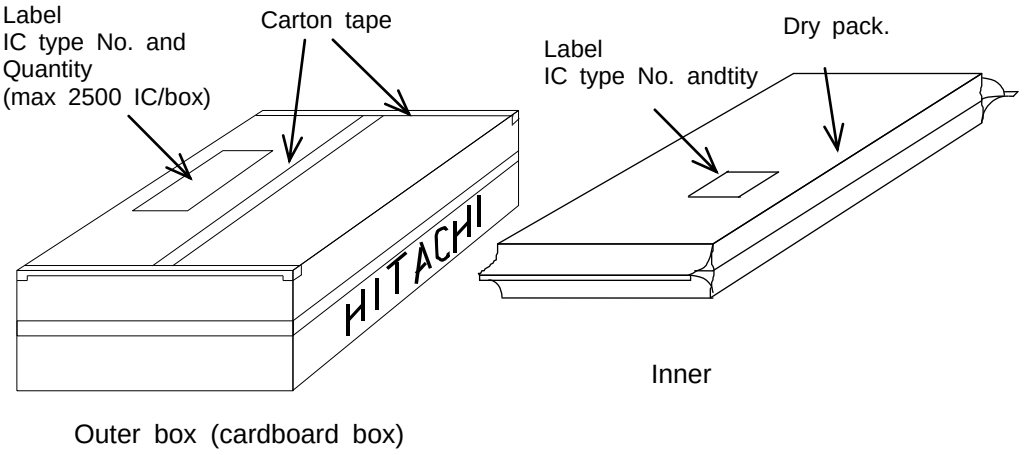
(c),(d),(e) :Serial number within year/month code

(f) to (o) : Parts name “ECN32910” or “ECN32911”

11 Packing Form

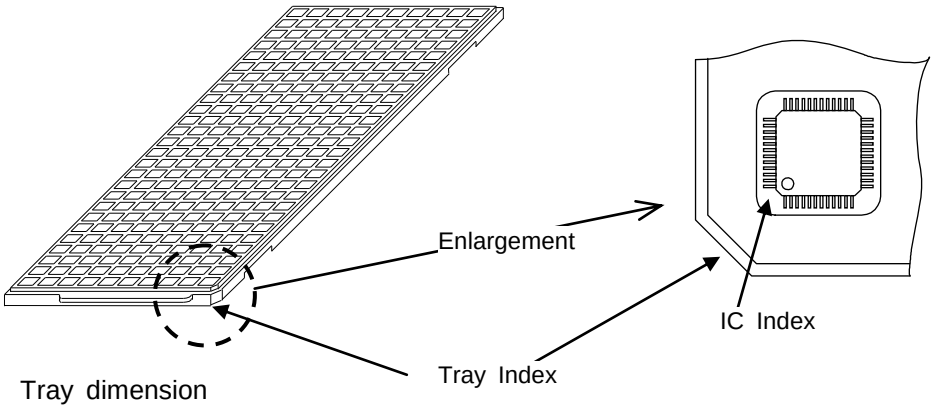
Packaging details are as shown below.

1.Outer and inner packing



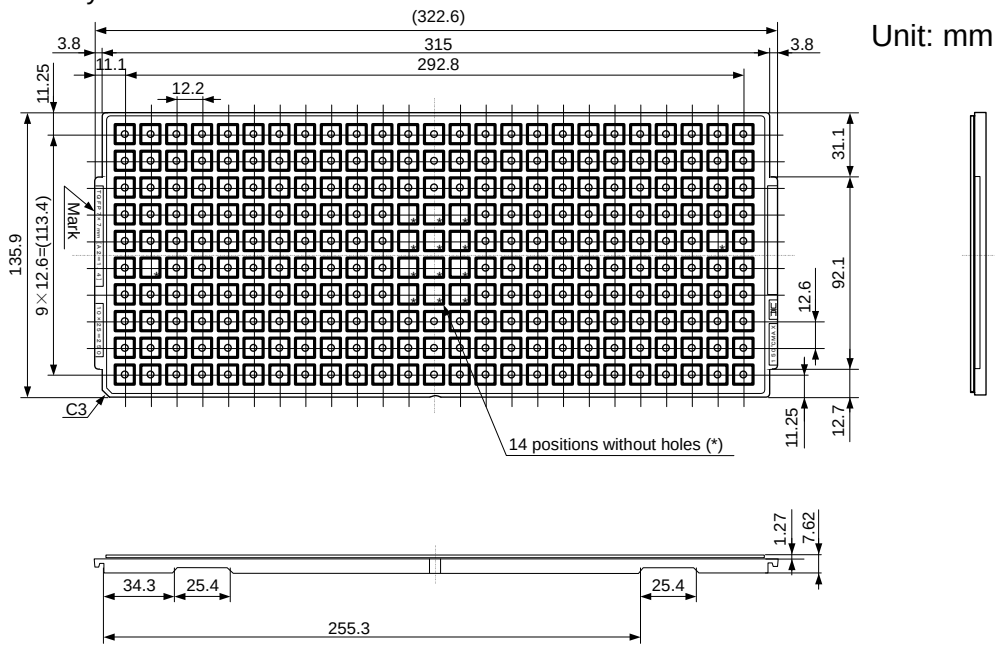
2.Tray

Tray Specifications
Orientation of IC



Tray dimension

Unit: mm



(1) Material of tray is PPE containing carbon and static proof.
(2) Packing quantity is max 250 IC/Tray.
(3) Maximum heat resistant temperature is 150deg.

12 Inspection

Hundred percent inspections shall be conducted on electric characteristics.

13 Important Notice

13.1 Hitachi warrants performance of its power semiconductor products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent Hitachi needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

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14 Cautions

14.1 Customers are advised to follow the below cautions to protect semiconductor from electrical static discharge (ESD).

a) IC needs to be dealt with caution to protect from damage by ESD. Material of container or any device to carry semiconductor devices should be free from ESD which may be caused by vibration while transportation. To use electric-conductive container or aluminum sheet is recommended as an effective countermeasure.

b) Those what touch semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.

c) Workers should be grounded connecting with high impedance around 100kΩ to 1MΩ while dealing with semiconductor to avoid damaging IC by electric static discharge.

d) Friction with other materials such as a high polymer should not be caused.

e) Attention is needed so that electric potential will be kept on the same level by short circuit terminals when PC board with mounted IC is carried and that vibration or friction might not occur.

f) Air conditionings needed so that humidity should not drop.

14.2 Refer to “Precautions for Use of High-Voltage Monolithic ICs” for the other precautions and instructions on how to deal with products.

14.3 Regardless of changes in external conditions during use, “absolute maximum ratings” should never be exceeded in designing electronic circuits that employ products. In a case absolute maximum ratings are exceeded, products may be damaged or destroyed. In no event shall Hitachi be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

14.4 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

14.5 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment).
Inclusion of products in such application shall be fully at the risk of customers. Hitachi, Ltd. assumes no liability for applications assistance, customer product design, or performance.
In such cases it is advised customers ensure circuit and/or product safety by using semiconductor devices that assures high reliability or by means of user’s fail-safe precautions or other arrangement.
(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

14.6 Lead-free solder is used for coating pins and the tab of this IC. Refer to "Precautions for Use of High-Voltage Monolithic ICs” for soldering conditions.

◆Appendix-Supplementary Data

Please read below contents before using this product.

Function Description

1. Bleed resistor
   ECN32911TF feature integrated 35kΩ bleed resistor to discharge capacitive Loads such as piezoelectric transducers. Each analog switch terminal is connected RGND with a bleed resistor.

2. Power supply sequence
   ECN32910TF/32911TF doesn't require the power up/down special sequence of the VDC and VDD power supplies.
   However, shift register and latch are unsettled just after power-up.
   Therefore, it's necessary to set the data of shift register after power-up.
   (Please refer to the truth table. : Table.6)

Precautions for Safe Use and Notices

If semiconductor devices are handled inappropriate manner, failures may result. For this reason, be sure to read "Precaution for Use" before use.

⚠ This mark indicates an item about which caution is required.

⚠ **CAUTION** This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

⚠ CAUTION

(1) Regardless of changes in external conditions during use "absolute maximum ratings" should never be exceed in designing electronic circuits that employ semiconductors. In the case of pulse use, furthermore,″safe operating area (SOA)"precautions should be observed.

(2) Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

(3) In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user's fail-safe precautions or other arrangement. Or consult Hitachi's sales department staff.

(If a semiconductor devices fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst)

NOTICES

1. This Development Target specification contains the specifications, characteristics (in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called "products") to aid in the selection of suitable products.
2. The specifications and dimensions, etc. stated in this Development Target specification are subject to change without prior notice to improve products characteristics. Before ordering, purchasers are advised to contact Hitachi's sales department for the latest version of this Development Target specification and specifications.
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