

# ECN33101SP/SPR/SPV

## 1. Product Description

### 1.1 Description

- (1) A motor is driven by three input signals (U, V, W) to ECN33101.
- (2) Dead time and six control signals from three input signals are generated in ECN33101.
- (3) Applicable to three shunt motor control method because emitter pins are set for U, V, W of bottom arm IGBTs (Insulated Gate Bipolar Transistors).
- (4) Acceptable for incoming power of AC 100V to 115V. Maximum rating: 250VDC/1.4A.
- (5) Latch-up free monolithic IC built with high voltage Dielectric Isolation (DI) technology.

### 1.2 Functions and Features

- (1) Three input type.
- (2) Built-in dead time generation. (Top and bottom arm short-circuit protection)
- (3) Three shunt method applicable.
- (4) IGBT all off signal input pin.
- (5) Fault output pin.
- (6) Built-in charge pump circuit.
- (7) Built-in 5V power supply circuit.
- (8) Built-in over-current protection.
- (9) Built-in 15V\_VCC under-voltage detection.

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## 1.3 Block Diagram

ECN33101 is shown inside the bold line in Fig. 1.1.

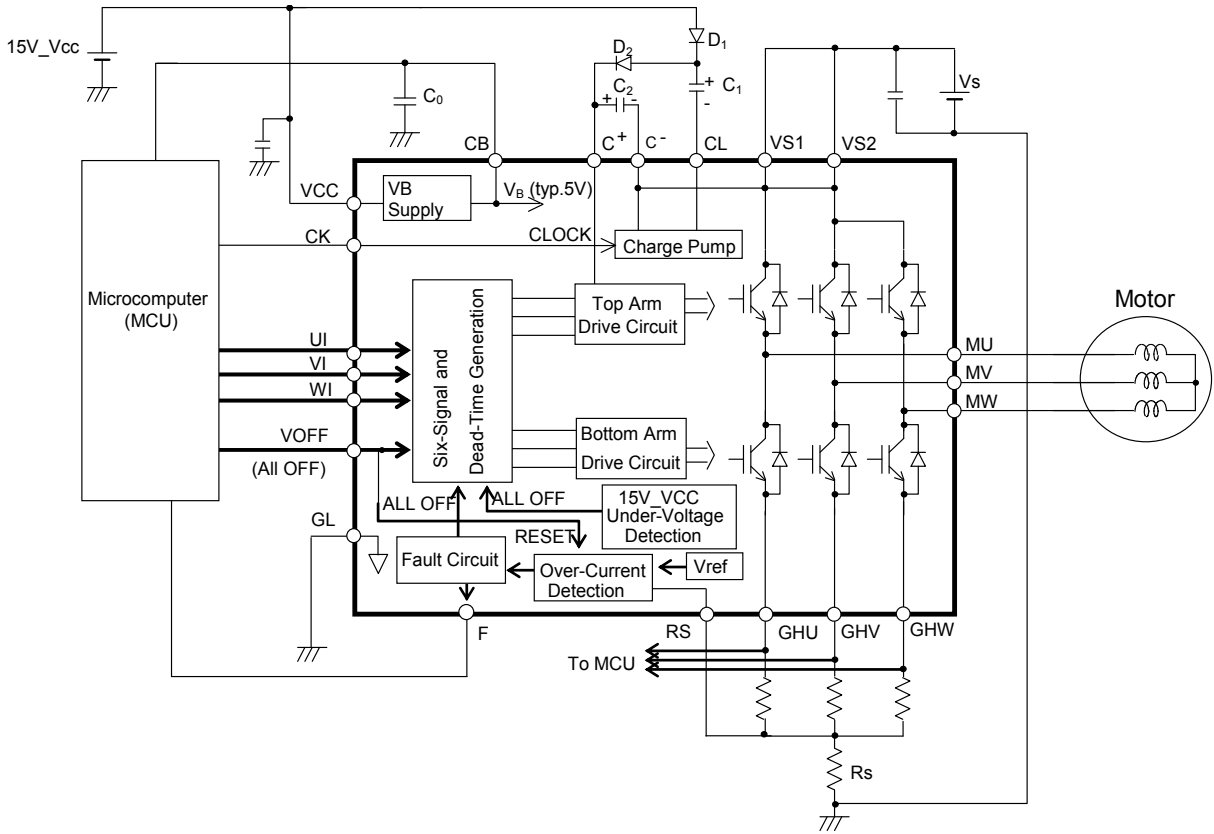
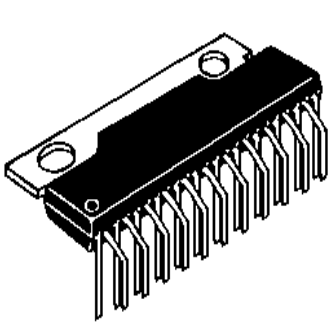
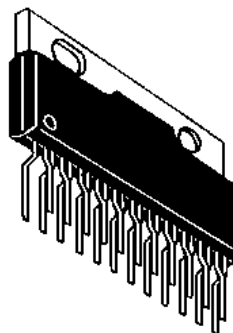


Fig.1.1 Block Diagram

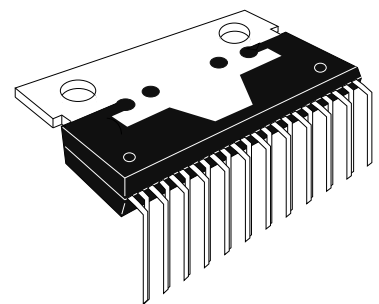
## 1.4 Types and Packages



ECN33101SP  
(Package Type:SP-23TA)



ECN33101SPV  
(Package Type:SP-23TB)



ECN33101SPR  
(Package Type:SP-23TR)

Fig. 1.2 Types and Packages of ECN33101

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## 2. Specifications

### 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute Maximum Ratings**

Condition: Ta=25°C

No.	Item	Symbol	Pin	Rating	Unit	Condition	
1	Output device breakdown voltage	VSM	VS1, VS2 MU, MV, MW	250	V		
2	VCC power supply voltage	15V_VCC	VCC	18	V		
3	Voltage between C+ and C-	VCPM	C+, C-	18	V		
4	Input voltage	VIN	UI, VI, WI CK, RS, VOF F	-0.5 to VB+ 0.5	V		
5	Output current	Pulse	IP	MU, MV, MW	1.4	A	Note 1
6		DC					
7	VB supply output current	IBMAX	CB	50	mA		
8	Junction operating temperature	Tjop	—	-20 to +135	°C	Note 2	
9	Storage temperature	Tstg	—	-40 to +150	°C		

Note 1: Output IGBTs can handle this peak current at 25 °C junction operating temperature.

Note 2: Thermal resistance

(1) Between junction and ECN33101 case (tab): Rjc=4 °C/W

(2) Between junction and air: Rja=40 °C/W

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## 2.2 Electrical Characteristics

**Table 2.2 Electrical Characteristics** Suffix (T: Top arm, B: Bottom arm) Condition: Ta=25°C

No.	Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Condition	
1	Standby current	ISH	VS1, VS2	—	0.15	1.00	mA	VOFF=0V, CK=0V VS=141V, VCC=15V, IB=0A	
2		ICC	VCC	—	3	10	mA		
3	IGBT collector-emitter saturation voltage	VONT	MU, MV, MW	—	2.0	3.0	V	I=0.7A, VCC=15V	
4		VONB	MU, MV, MW	—	2.0	3.0	V		
5	Output delay time	Turn on	TdONT	MU, MV, MW	—	2.0	3.0	μs	VS=141V, VCC=15V I=0.7A Resistive load
6			TdONB	MU, MV, MW	—	2.0	3.0	μs	
7		Turn off	TdOFFT	MU, MV, MW	—	1.0	2.0	μs	
8			TdOFFB	MU, MV, MW	—	1.0	2.0	μs	
9	Dead time	Top arm on	TDT	MU, MV, MW	0.3	1.0	1.8	VS=141V, VCC=15V, I=0.7A Resistive load Note 1	
10		Bottom arm on	TDB	MU, MV, MW	0.3	1.0	1.8		μs
11	Free-wheeling diode forward voltage	VFDT	MU, MV, MW	—	2.0	2.5	V	I=0.7A	
12		VFDB	MU, MV, MW	—	2.0	2.5	V		
13	Over current protection reference voltage	Vref	RS	0.45	0.50	0.55	V	VCC=15V	
14	Over current protection delay time	Tref	RS	—	4.0	6.0	μs	VCC=15V	
15	UI, VI, WI, VOFF, CK inputs	Voltage	VIH	UI, VI, WI, VOFF, CK	2.5	—	—	V	VCC=15V
16			VIL	UI, VI, WI, VOFF, CK	—	—	1.0	V	
17		Current	IIL	UI, VI, WI, VOFF, CK	-10	—	—	μA	Input =0V VCC=15V Pull-down resistor Note 2
18			IiH	UI, VI, WI, VOFF, CK	—	—	100	μA	
19	RS input current	IILRS	RS	-100	—	—	μA	RS=0V Pull-up resistor Note 3	
20	VB supply output	Voltage	VB	CB	4.5	5.0	5.5	V	VCC=15V, IB=0A
21		Current	IB	CB	—	—	45	mA	
22	LVSD	Operating voltage	LVSDON	VCC, MU, MV, MW	11.0	11.7	12.5	V	Note 4
23		Recovery voltage	LVSDOFF	VCC, MU, MV, MW	11.5	12.2	13.0	V	
24	F output resistance	ROP	F	—	2.0	4.0	kΩ	I=1mA, VCC=15V Note 5	
25		RON	F	—	0.7	1.5	kΩ		
26	Fault reset delay time	tfirs	F	—	15	30	μs	VCC=15V	
27	All off delay time	taoff	VOFF	—	2.0	4.0	μs	VCC=15V	

Note 1: The definition of dead time is shown in Fig. 2.4. The values of No.9 and No.10 are based on actual measurement values. Therefore, not all values of No.9 and No.10 are the same as the values calculated from the values of No.5 to No.8.

Note 2: Internal pull-down resistances are typically 200kΩ. Fig. 2.1 is the equivalent circuit.

Note 3: Internal pull-up resistance is typically 200kΩ. Fig. 2.2 is the equivalent circuit.

Note 4: The LVSD function detects and shuts down at low VCC.

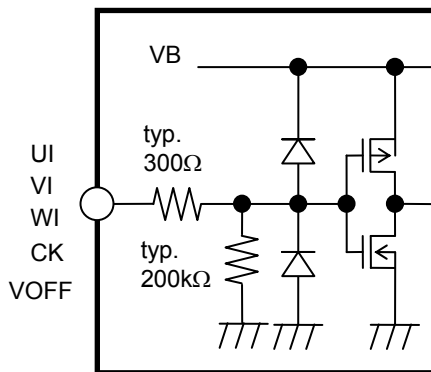
Note 5: The equivalent circuit is shown in Fig. 2.3.

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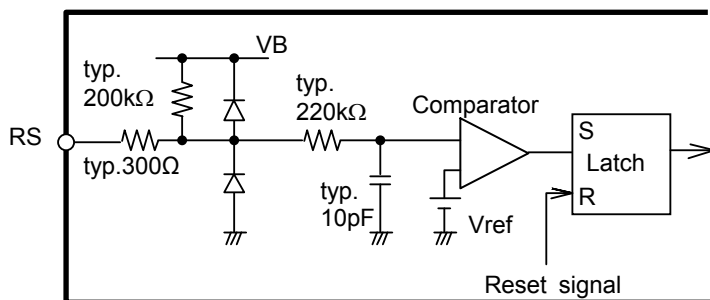
## 2.3 Operating Condition

**Table 2.3 Operating Condition**

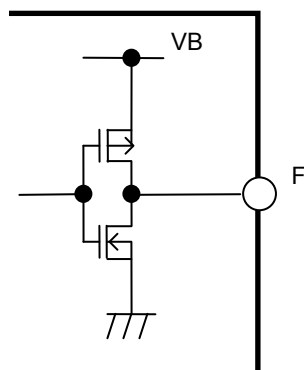
No.	Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Condition
1	Supply voltage	VSop	VS1, VS2	15	—	185	V	
2		VCCop	VCC	13.5	15.0	16.5	V	
3	Clock input frequency	Fck	CK	12	—	22	kHz	
4	PWM input frequency	Fpwm	UI, VI, WI	12	—	22	kHz	
5	GH voltage	Vgh	GHU, GHV, GHW	-1.0	—	1.0	V	Based on GL



**Fig. 2.1 Equivalent Circuit Around UI, VI, WI, CK, VOFF Pins**



**Fig. 2.2 Equivalent Circuit Around RS Pin**



**Fig. 2.3 Equivalent Circuit Around F Pin**

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## 2.4 Functions and Operations

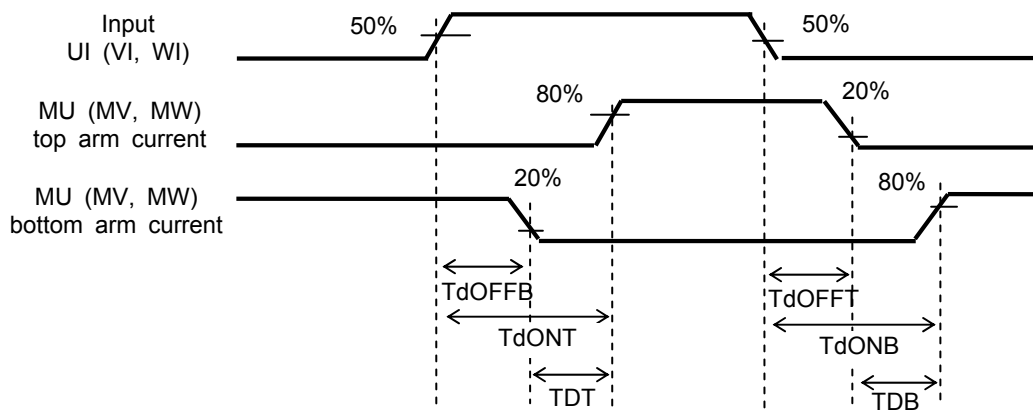
### 2.4.1 Truth Table

**Table 2.4 Truth Table**

Pin	Input	Top arm	Bottom arm
UI, VI, WI	L	OFF	ON
	H	ON	OFF
VOFF	L	ALL OFF	
	H	Based on UI, VI, WI inputs	

### 2.4.2 Dead Time

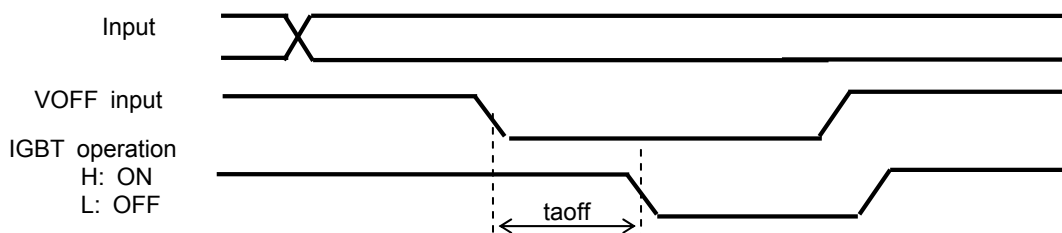
The ECN33101 generates six signals with dead time from three input signals, and the six signals control top and bottom arm IGBTs.



**Fig. 2.4 Definition of Dead Time (Resistive Load)**

### 2.4.3 All Output IGBT Shutoff Function

When "L" is input to VOFF pin, all IGBTs are turned off. When "H" is input to VOFF pin, IGBTs operate based on UI, VI, WI, and RS input signals.



**Fig. 2.5 Definition of taoff**

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## 2.4.4 Over Current Protection

The ECN33101 monitors the current through the shunt resistance  $R_s$ . When the voltage at the RS pin exceeds the  $V_{ref}$  ( $V_{ref}$  is Typically 0.5V) of the internal detection circuit, all IGBTs are turned off and the F pin outputs "L". Input "L" at VOFF pin to reset this all off state. The F pin outputs "H" by inputting "L" after a lapse of fault reset delay time ( $t_{flrs}$ ). Lengthen the period of VOFF "L" for the fault reset delay time or more.

Input "H" at VOFF pin to restart.

Just after the 15V\_VCC is input, the over current protection may operate. In this case, reset the all off state.

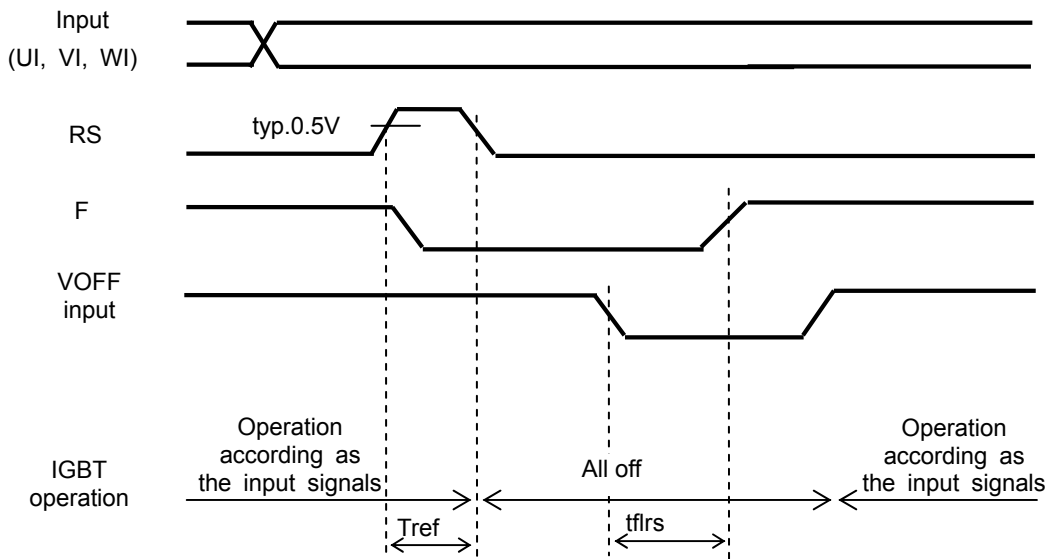


Fig. 2.6 Definition of Tref, tflrs

## 2.4.5 15V\_VCC Under-Voltage Detection

When the 15V\_VCC voltage goes below the LVSD operating voltage (LVSDON), all IGBTs are turned off.

When the 15V\_VCC voltage goes up, this all off state is reset at the LVSD recovery voltage (LVSDOFF).

## 2.4.6 Input Signals at Standby Condition

Input "L" at VOFF and CK pins at standby condition.

## 2.4.7 Clock Signal

Input the clock signal specified as follows into CK pin.

- H level =  $V_B$ , L level = 0V, Duty = 50%

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## 3. Specifications

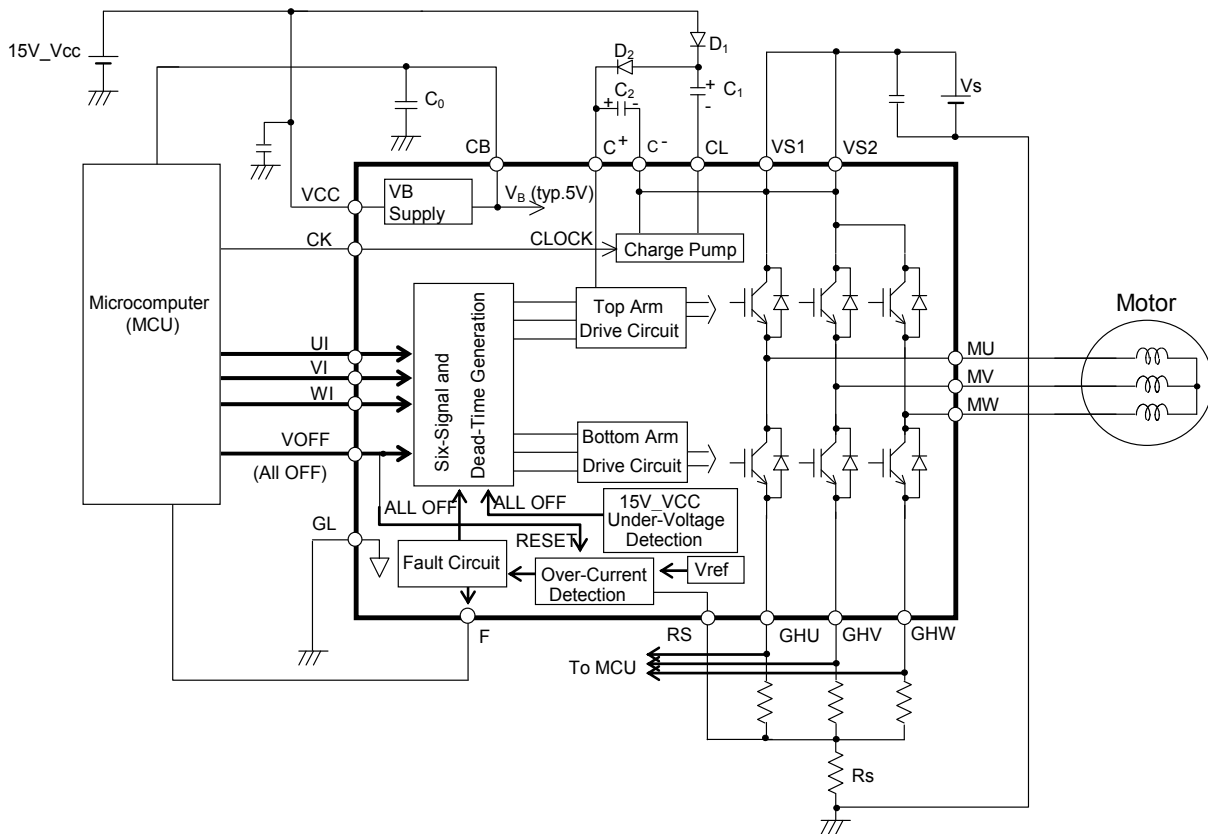
### 3.1 External Parts

**Table 3.1 External Parts**

Part	Standard Value	Usage	Remarks
C0	1.0μF ± 20%	Filters the internal power supply (VB)	Stress voltage is VB (=5.5V)
C1, C2	1.0μF ± 20%	For charge pump	Stress voltage is 15V_VCC
D1, D2	400V, 1.0A trr ≤100ns	For charge pump	
Rs	Note 1	Sets over current limit	

Note 1: The over current protection setting IO is calculated as follows.

$$IO = Vref / Rs \quad (A)$$



**Fig. 3.1 Block Diagram** (ECN33101 is shown inside the bold line.)

### 3.2 Input Pins (UI, VI, WI, VOFF, CK)

In some applications, input pins may be sensitive to noise due to high impedance.

If noise is detected at an input pin, the following resistor and /or capacitor should be added.

- Resistor : 5.6kΩ±5% pull-down resistor between the GL pin and input pins.
- Capacitor : 470pF±20% ceramic capacitor close to the input pins (UI, VI, WI, CK).  
: 0.01μF±20% ceramic capacitor close to the input pin (VOFF).



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## 4. Pin Locations

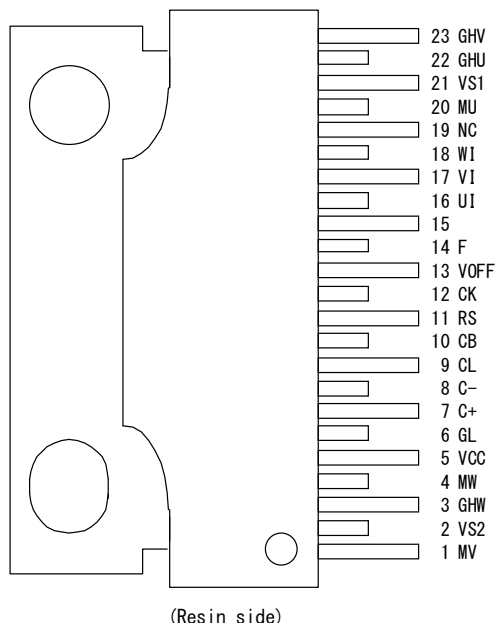


Fig. 4.1 Pin Locations

## 5. Explanations of Pins

Table 5.1 Explanations of Pins

No.	Symbol	Definition	Remarks
1	MV	V phase output	Note 1
2	VS2	Power supply for top arm IGBTs of V and W phases	Note 1, Note 2
3	GHW	Emitter of W phase bottom arm IGBT and anode of W phase bottom arm FWD	
4	MW	W phase output	Note 1
5	VCC	15V control power supply	
6	GL	Control system GND	
7	C+	For the charge pump circuit, power supply for top arm drive circuits	Note 1
8	C-	For the charge pump circuit	Note 1, Note 2
9	CL	For the charge pump circuit	Note 1
10	CB	5V power supply output	
11	RS	RS voltage input for over current protection	
12	CK	Clock input	
13	VOFF	All off input	
14	F	Fault signal output	
15	—	Feedback signal output for kit product (ECN39100 series) Open the pin.	
16	UI	Input control signal for U phase	
17	VI	Input control signal for V phase	
18	WI	Input control signal for W phase	
19	NC	No connection	Note 3
20	MU	U phase output	Note 1
21	VS1	Power supply for top arm IGBT of U phase	Note 1, Note 2
22	GHU	Emitter of U phase bottom arm IGBT and anode of U phase bottom arm FWD	
23	GHV	Emitter of V phase bottom arm IGBT and anode of V phase bottom arm FWD	

Note 1: High voltage pin.

Note 2: The VS1, VS2 and C- pins are connected within the ECN33101 but VS1 and VS2 must also be connected by external wiring.

Note 3: Not connected to the internal chip.

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## 6. Inspection

Hundred percent inspection is conducted on electric characteristics at  $T_a = 25 \pm 5^\circ\text{C}$ .

## 7. Warnings and Usage Precautions

### 7.1 Assembling

When assembling the device on the heat sink, tightening torque range should be 0.39 to 0.78N·m.  
Tab should not be soldered.

### 7.2 Countermeasure Against Electrical Static Discharge (ESD)

- (a) The ECN33101 must be handled carefully to protect it from ESD. The material of containers or any other device used to carry semiconductor devices should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
- (b) Everything that touches semiconductor devices, such as the work platform, machine, measuring equipment, and test equipment should be grounded.
- (c) Workers should be high-impedance grounded (around 100k $\Omega$  to 1M $\Omega$ ) while working with the semiconductor, to avoid damaging the ECN33101 by ESD.
- (d) Friction with other materials, such as high polymers, should be avoided.
- (e) When a PCB with a mounted ECN33101 is carried, ensure that electric potential is kept on the same level by the short-circuit terminals and that vibration or friction does not occur.
- (f) The humidity at assembly line to mount IC on circuit boards should be kept around 45 to 75 percents using humidifiers or such. If the humidity cannot be controlled sufficiently, using neutralization apparatus such as ionizers are effective.

### 7.3 Note regarding Insulation between Pins

High voltages are applied between the pin numbers specified below. Hitachi advises the application of coating resin or molding treatment.

Between pin numbers: 1 - 2, 2 - 3, 3 - 4, 4 - 5, 6 - 7, 8 - 9, 9 - 10, 18 - 20, 20 - 21, 21 - 22

### 7.4 Output Short-Circuit Protection

ECN33101 has no protection function against output short-circuit (load short-circuit, earth fault, etc.). If output is short-circuited, there is a possibility that the ECN33101 will be destroyed. Thus, be sure to protect it externally.

### 7.5 Absolute Maximum Ratings

Regardless of changes in external conditions during use, "absolute maximum ratings" should never be exceeded in designing electronic circuits that employ the ECN33101. If absolute maximum ratings are exceeded, the ECN33101 may be damaged or destroyed. In no event shall Hitachi be liable for any failure in the ECN33101 or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

### 7.6 Derating Design

Continuous high-loaded (high temperature, high voltage, large current) operation should be avoided and derating design should be applied, even within the ranges of the absolute maximum ratings, to ensure reliability.

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## 7.7 Safe Design

The ECN33101 may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.

## 7.8 Use

The ECN33101 is not manufactured to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment).

Inclusion of the ECN33101 in such application shall be fully at the risk of the customer. Hitachi assumes no liability for applications assistance, customer product design, or performance.

In such cases customers are advised to ensure circuit and/or product safety by using semiconductor devices that assures high reliability or by user's fail-safe precautions or other arrangements. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

## 7.9 Soldering

The peak temperature of flow soldering\* must be less than 260°C, and the dip time must be less than 10 seconds. High stress by mounting, such as long time thermal stress by preheating, mechanical stress, etc, can lead to degradation or destruction. Make sure that your mounting method does not cause problem as a system.

\* Flow soldering: Only pins enter a solder bath, while the resin or tab does not.

## 7.10 Other

See the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for other precautions and instructions on how to deal with these kinds of products.

## 8. Operation

- (1) Hitachi warrants performance of the ECN33101 to the specifications applicable at the time of sale in accordance with this specification. Testing and other quality control techniques are utilized to the extent Hitachi needs to meet specifications described in this document. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.
- (2) If the performance of the ECN33101 does not meet this specification within one month after the delivery, all of the appropriate lot will be tested and delivered again. However, the ECN33101 delivered more than one month ago is excluded.
- (3) Hitachi assumes no obligation for compensation for any fault in customer's goods using the ECN33101 in the marketplace. However, if Hitachi clearly has a responsibility and the ECN33101 does not meet this specification, and a customer demands for compensation within one year after the delivery of the ECN33101, the customer will be compensated by substitutions or amount of money up to worth of them.

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- (4) Hitachi reserves the right to make changes in this specification and to discontinue mass production of the ECN33101 without notice. Customers are advised before purchasing to confirm that this specification of the ECN33101 is the latest version and that the ECN33101 is on mass-production status if purchasing has been suspended for one year or more.
- (5) In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user's units according to this specification. Hitachi assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in this specification.
- (6) No license is granted by this specification under any patents or other rights of any third party or Hitachi Power Semiconductor Device, Ltd.
- (7) This specification should not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of Hitachi Power Semiconductor Device, Ltd.
- (8) For the ECN33101 (technologies) described in this specification, the followings are prohibited.
- (a) To provide to any party whose purpose in their application will hinder maintenance of international peace and safety.
  - (b) To be applied to the above-described purpose by direct purchasers or any third party.  
When exporting the ECN33101 (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

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## Supplementary Reference Data

Refer to the derating information below when designing with the ECN33101.

### 1. Safe Operation Area (SOA)

It is important that the ECN33101 be used within the SOA shown in Fig. 1.1, where the current and voltage are at the MU, MV, and MW pins (motor coils).

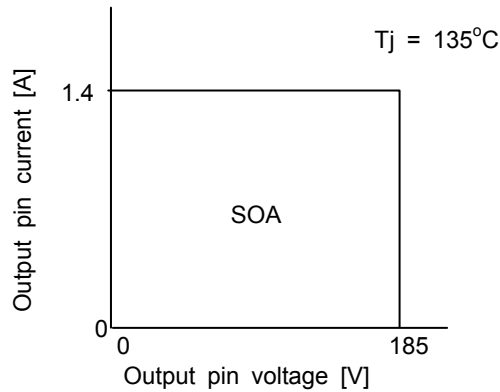


Fig. 1.1 SOA

### 2. General Design Derating Standards

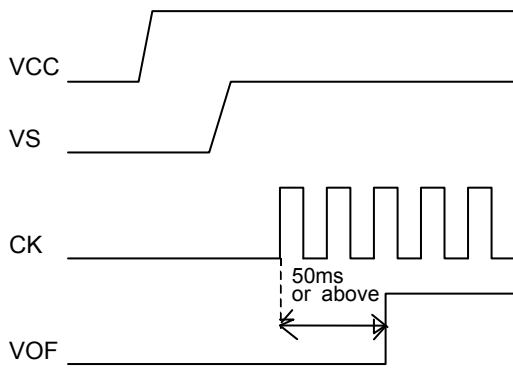
- (a) Temperature: Junction operating temperature must be kept under  $110^\circ\text{C}$ .
- (b) Supply voltage: VS power supply voltage must be kept under 185V.

### 3. Power Supply Sequence

Follow the power supply sequence below.

- At the time of power on ; Power on VCC → Power on VS → Input clock to CK pin → Input “H” at VOFF pin
- At the time of power off ; Input “L” at VOFF pin → Stop inputting clock to CK pin → Power off VS → Power off VCC

At the time of power on



At the time of power off

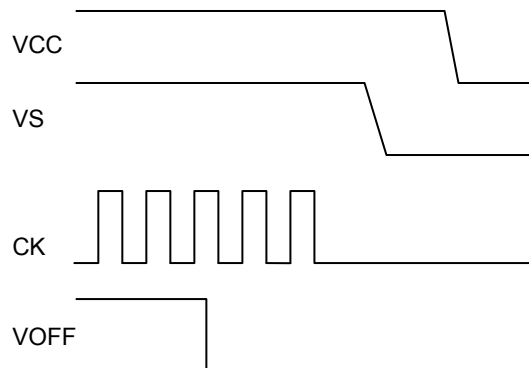


Fig. 3.1 Power Supply Sequence at Time of Power On

Fig. 3.2 Power Supply Sequence at Time of Power Off

# ECN33101SP/SPR/SPV

## 4. Dimensions (mm)

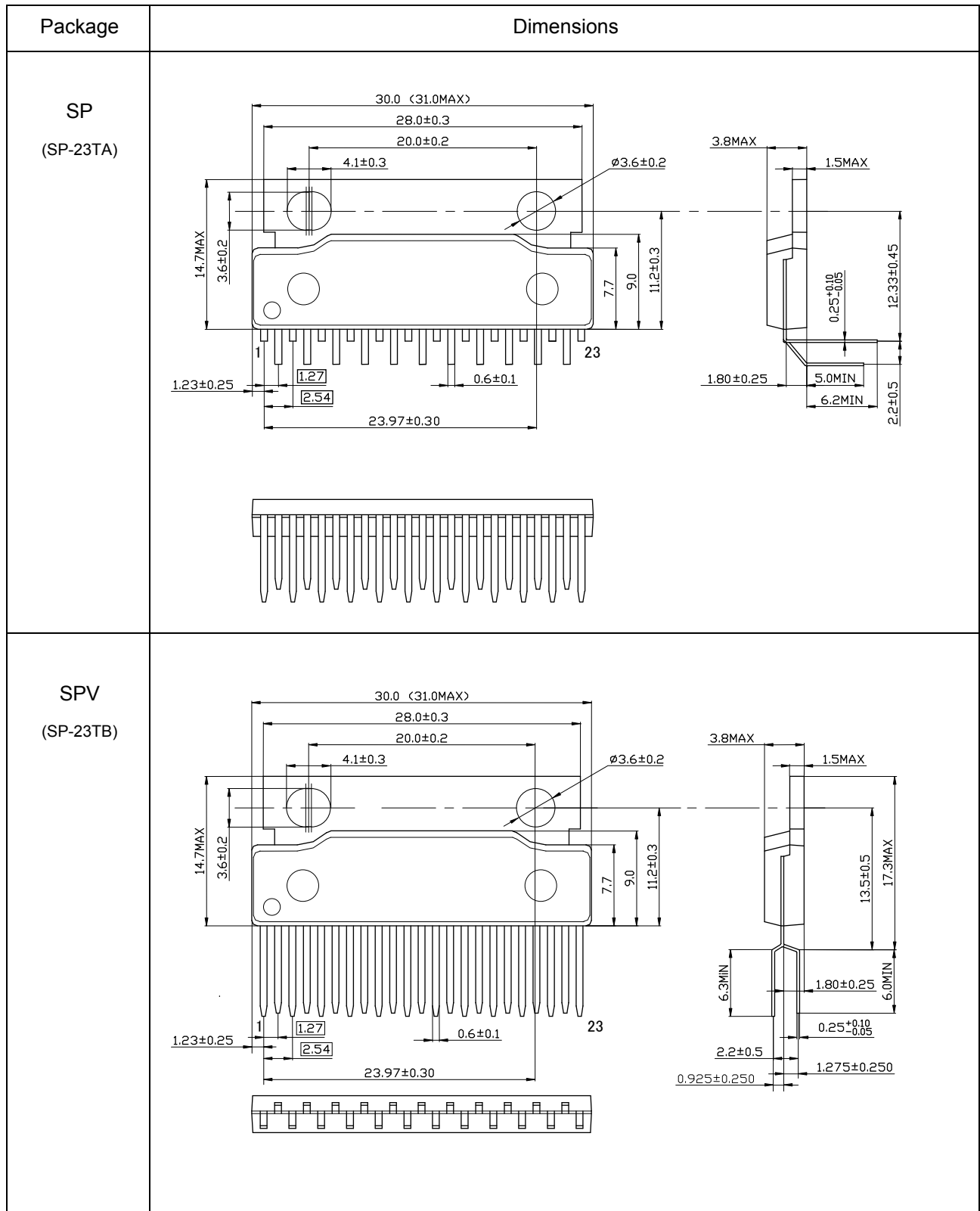


Fig. 4.1 Dimensions (SP, SPV) (mm)

# ECN33101SP/SPR/SPV

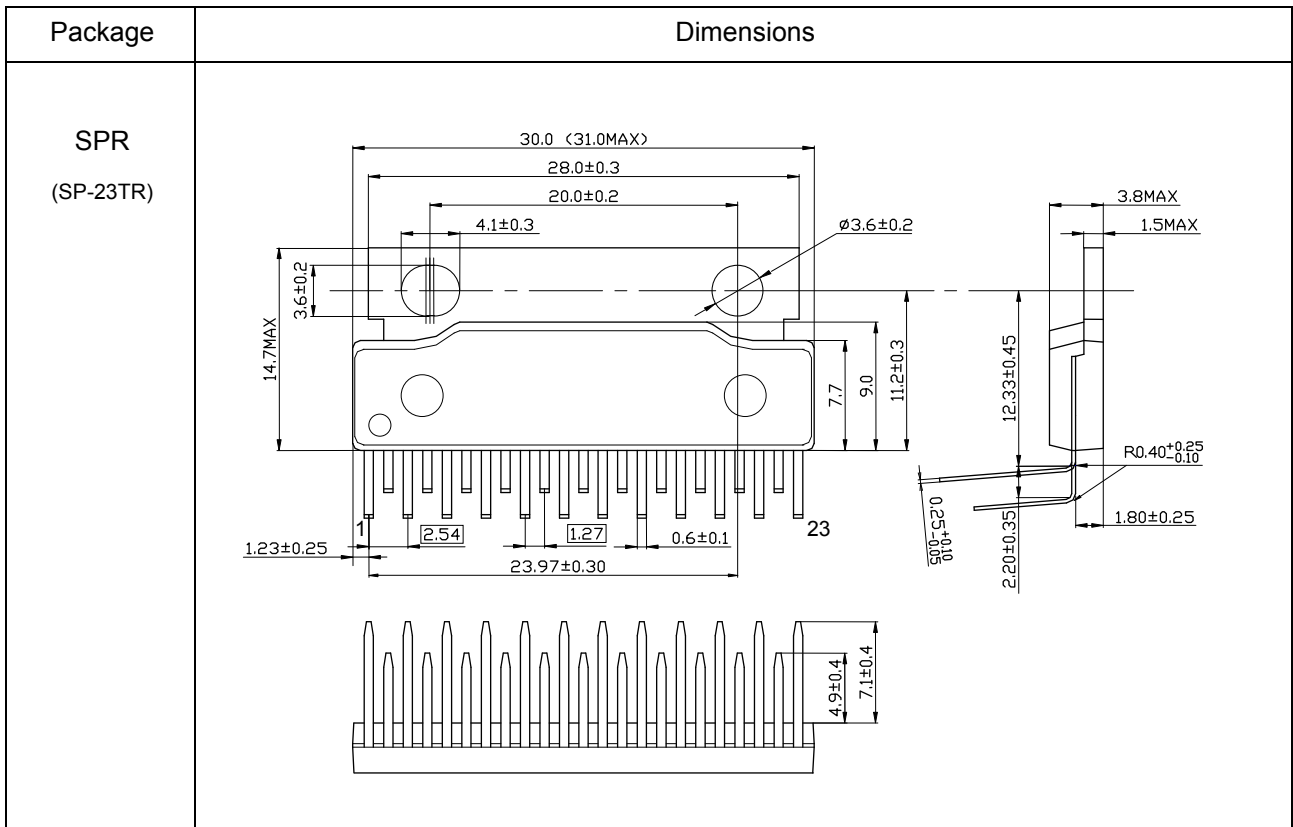


Fig. 4.2 Dimensions (SPR) (mm)

## Precautions for Safe Use and Notices

If semiconductor devices are handled in inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item about which caution is required.



### CAUTION

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.



### CAUTION

- (1) Regardless of changes in external conditions during use "absolute maximum ratings" should never be exceeded in designing electronic circuits that employ semiconductors. In the case of pulse use, furthermore, "safe operating area (SOA)" precautions should be observed.
- (2) Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.
- (3) In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user's fail-safe precautions or other arrangement. Or consult Hitachi's sales department staff.

(If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst)

## NOTICES

1. This Data Sheet contains the specifications, characteristics (in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called "products") to aid in the selection of suitable products.
2. The specifications and dimensions, etc. stated in this Data Sheet are subject to change without prior notice to improve products characteristics. Before ordering, purchasers are advised to contact Hitachi's sales department for the latest version of this Data Sheet and specifications.
3. In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user's units according to this Data Sheet. Hitachi assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in this Data Sheet.
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<http://www.hitachi-power-semiconductor-device.co.jp/en/>