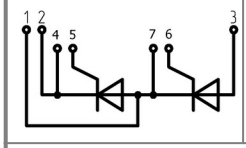
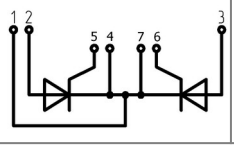
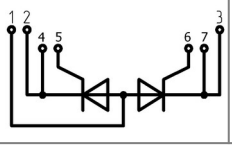
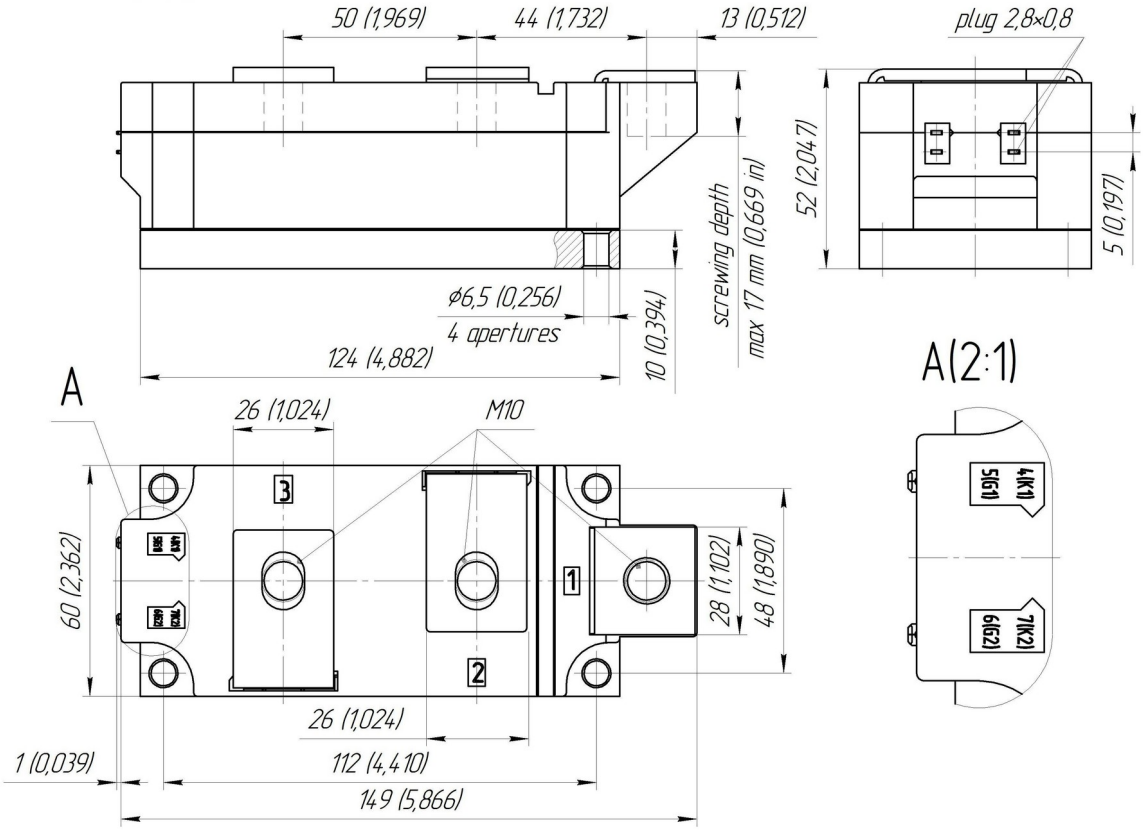
Electrically isolated base plate
Industrial standard package
Simplified mechanical design, rapid assembly
Pressure contact

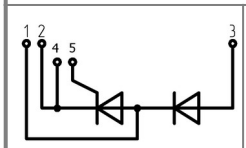
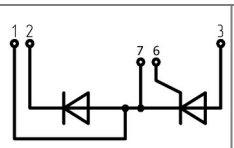
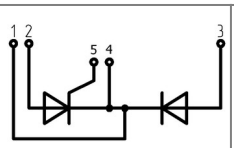
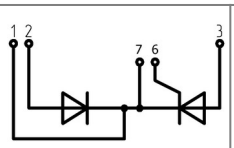
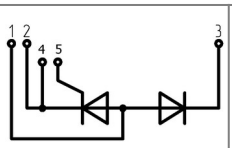
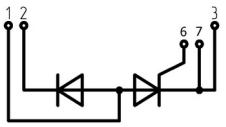
Double Thyristor Module For Phase Control MTx-430-24-A2

Mean on-state current		I_{TAV}	430 A
Repetitive peak off-state voltage		V_{DRM}	2000 ÷ 2400 V
Repetitive peak reverse voltage		V_{RRM}	
Turn-off time		t_q	250 µs
V_{DRM}, V_{RRM}, V	2000	2200	2400
Voltage code	20	22	24
T_j, °C	– 40 ÷ 125		

MT3		MT4		MT5	



MT/D3	MD/T3	MT/D4	MD/T4	MT/D5	MD/T5

All dimensions in millimeters (inches)

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	430	T_c=85 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	675		
I_{TSM}	Surge on-state current	kA	12.0 14.0	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			13.0 15.0	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s\cdot10^3$	720 980	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			700 930	$T_j=T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; $V_D=V_R$=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000÷2400	$T_{j\,min}< T_j <T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100÷2500	$T_{j\,min}< T_j <T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6\cdot V_{DRM}$ $0.6\cdot V_{RRM}$	$T_j=T_{j\,max}$; Gate open	
TRIGGERING					
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$	
V_{RGM}	Peak reverse gate voltage	V	5		
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current	
SWITCHING					
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	400	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥2 A/µs	
THERMAL					
T_{stg}	Storage temperature	°C	-40 ÷ 50		
T_j	Operating junction temperature	°C	-40 ÷ 125		
$T_{c\,op}$	Operating temperature	°C	-40 ÷ 125		
MECHANICAL					
a	Acceleration under vibration	m/s^2	50		

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.55	T_j=25 °C; I_{TM}=1256A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.00	T_j=$T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	0.410		
I_L	Latching current, max	mA	1000	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	100	T_j=$T_{j\,max}$; V_D=V_{DRM}; V_R=V_{RRM}	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/µs	1000	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00 2.50 2.00	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 200	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	µs	2.50	T_j=25 °C; V_D=1000 V; I_{TM}=I_{TAV}; di/dt=200 A/µs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs	
t_q	Turn-off time[2], max	µs	250	dv_D/dt=50 V/µs; T_j=$T_{j\,max}$; I_{TM}= I_{TAV}; di_R/dt=10 A/µs; V_R=100V; V_D=0.67 V_{DRM};	
THERMAL					
R_{thjc}	Thermal resistance, junction to case				
	per module	°C/W	0.0325	180° half-sine wave, 50 Hz	
	per arm	°C/W	0.0650		
	per module	°C/W	0.0310	DC	
	per arm	°C/W	0.0620		
R_{thch}	Thermal resistance, case to heatsink				
	per module	°C/W	0.0100		
	per arm	°C/W	0.0200		
INSULATION					
V_{ISOL}	Insulation test voltage	kV	3.00	Sine wave, 50 Hz; RMS	t=60 sec
			3.60		t=1 sec
MECHANICAL					
M_1	Mounting torque (M6)[3]	Nm	6.00	Tolerance ± 15%	
M_2	Terminal connection torque (M10)[3]	Nm	12.00	Tolerance ± 15%	
w	Weight, max	g	1500		

PART NUMBERING GUIDE

MT	3	-	430	-	24	-	A2	M2	-	A2	-	N
1	2		3		4		5	6		7		8

1. Thyristor module (MT)
   Thyristor – Diode module (MT/D)
   Diode – Thyristor module (MD/T)
2. Circuit Schematic:
   3 – serial connection
   4 – common Cathode
   5 – common Anode
3. Average On-state Current, A
4. Voltage Code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Package Type (M.A2)
8. Ambient Conditions:
   N – Normal

NOTES

1) Critical rate of rise of off-state voltage

Symbol of group	A2
$(dv_D/dt)_{crit}$, V/μs	1000

2) Turn-off time (dv_D/dt=50 V/μs)

Symbol of group	M2
t_q, μs	250

3) The screws must be lubricated

UL certified file-No. E255404

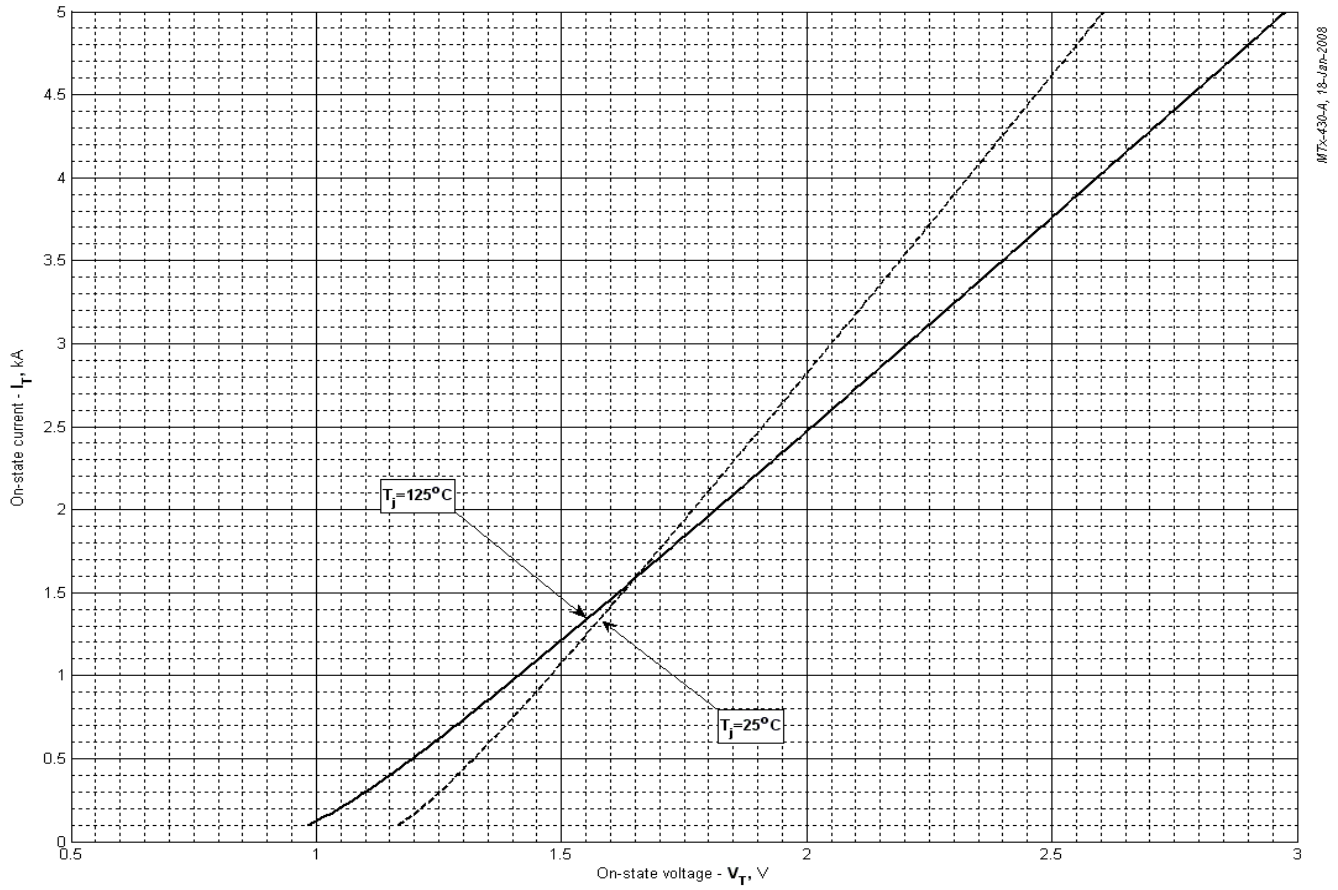


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	$T_j = T_{j\,max}$
A	1.069142	0.852344
B	0.239424	0.334163
C	-0.158239	-0.211339
D	0.278291	0.371677

On-state characteristic model (see Fig. 1)

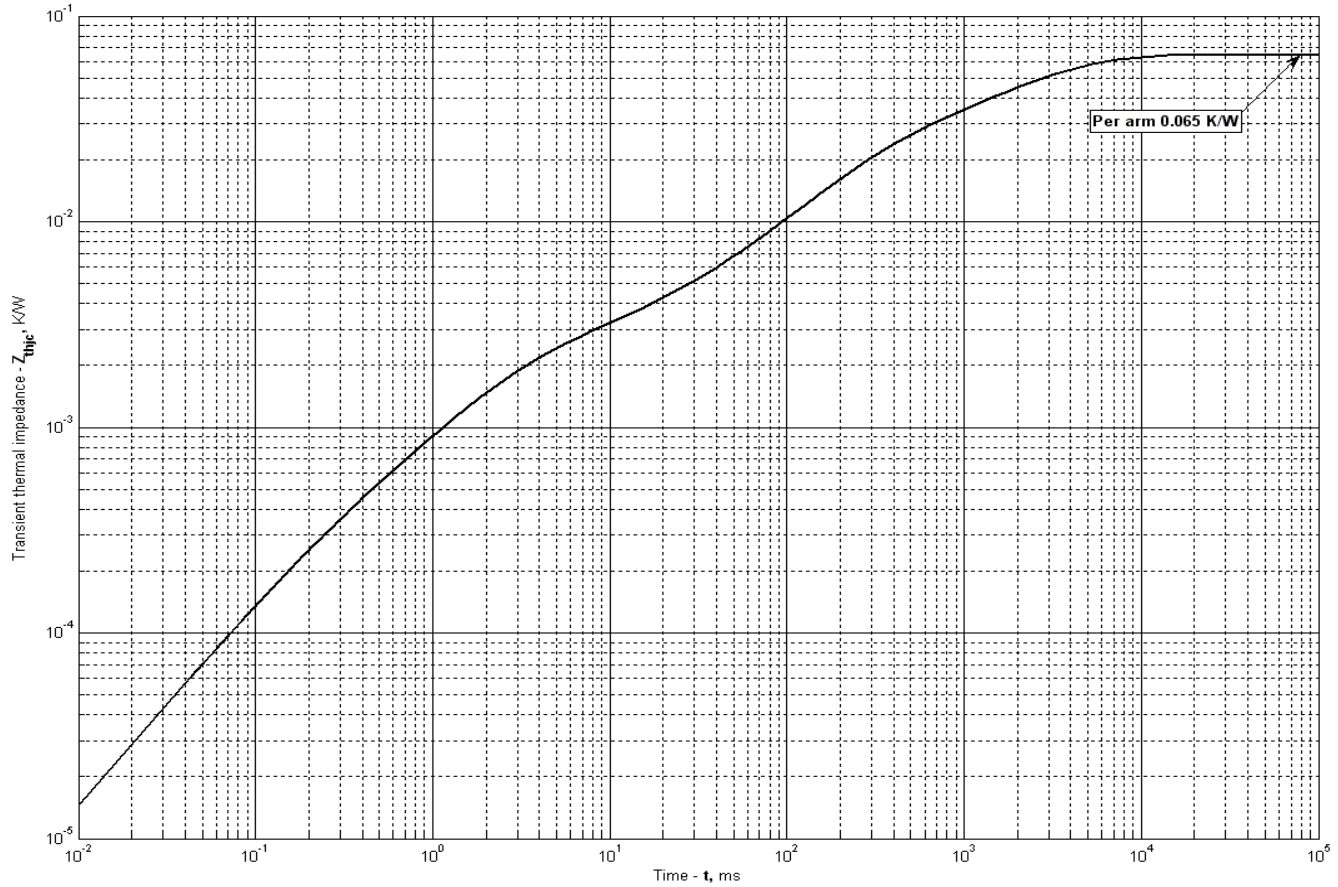


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.0344	0.0112	0.01635	0.0006528	0.001791	0.0001363
τ_i, **s**	3.132	1.000	0.2335	0.01038	0.002348	0.0002448

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

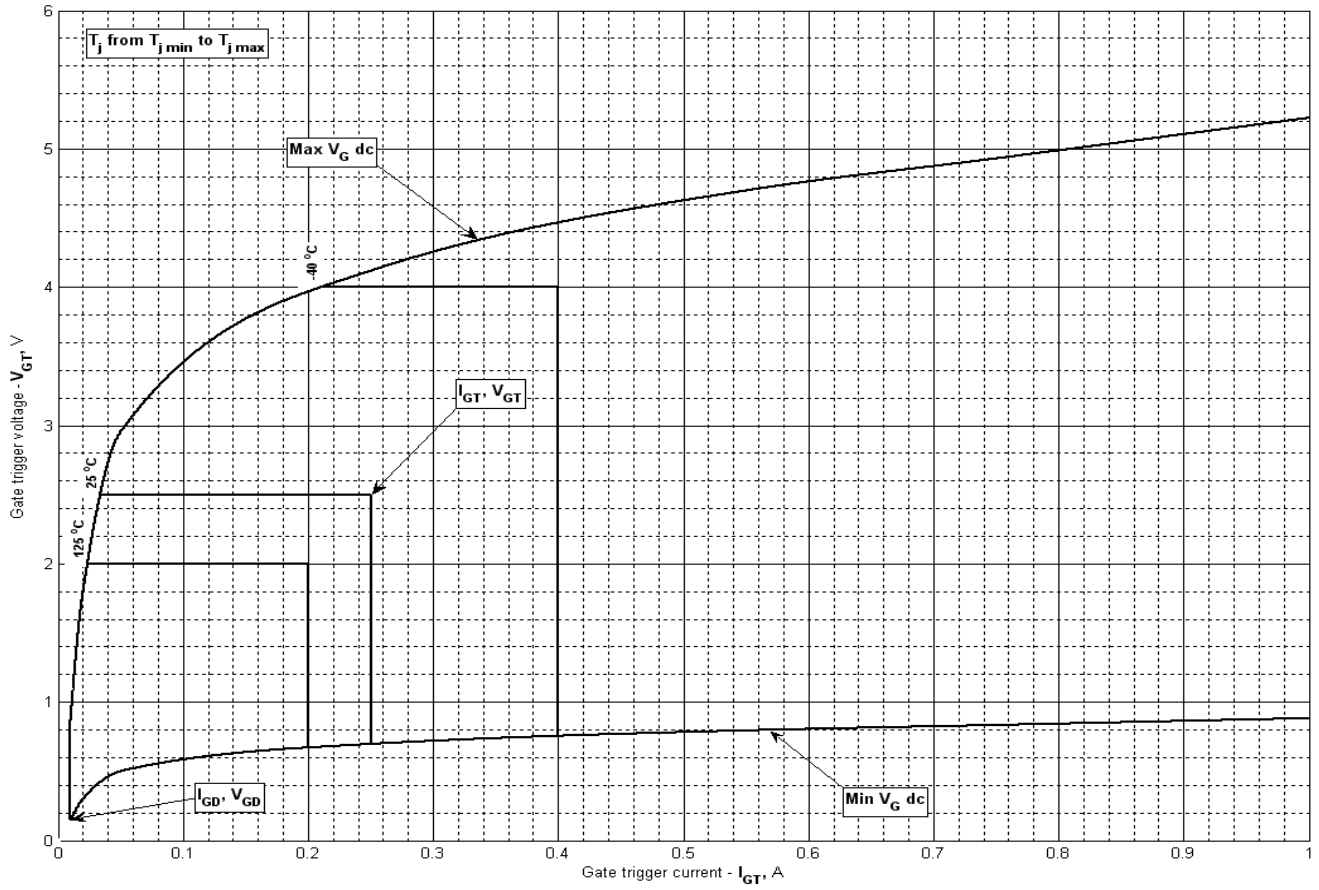


Fig 3 – Gate characteristics – Trigger limits

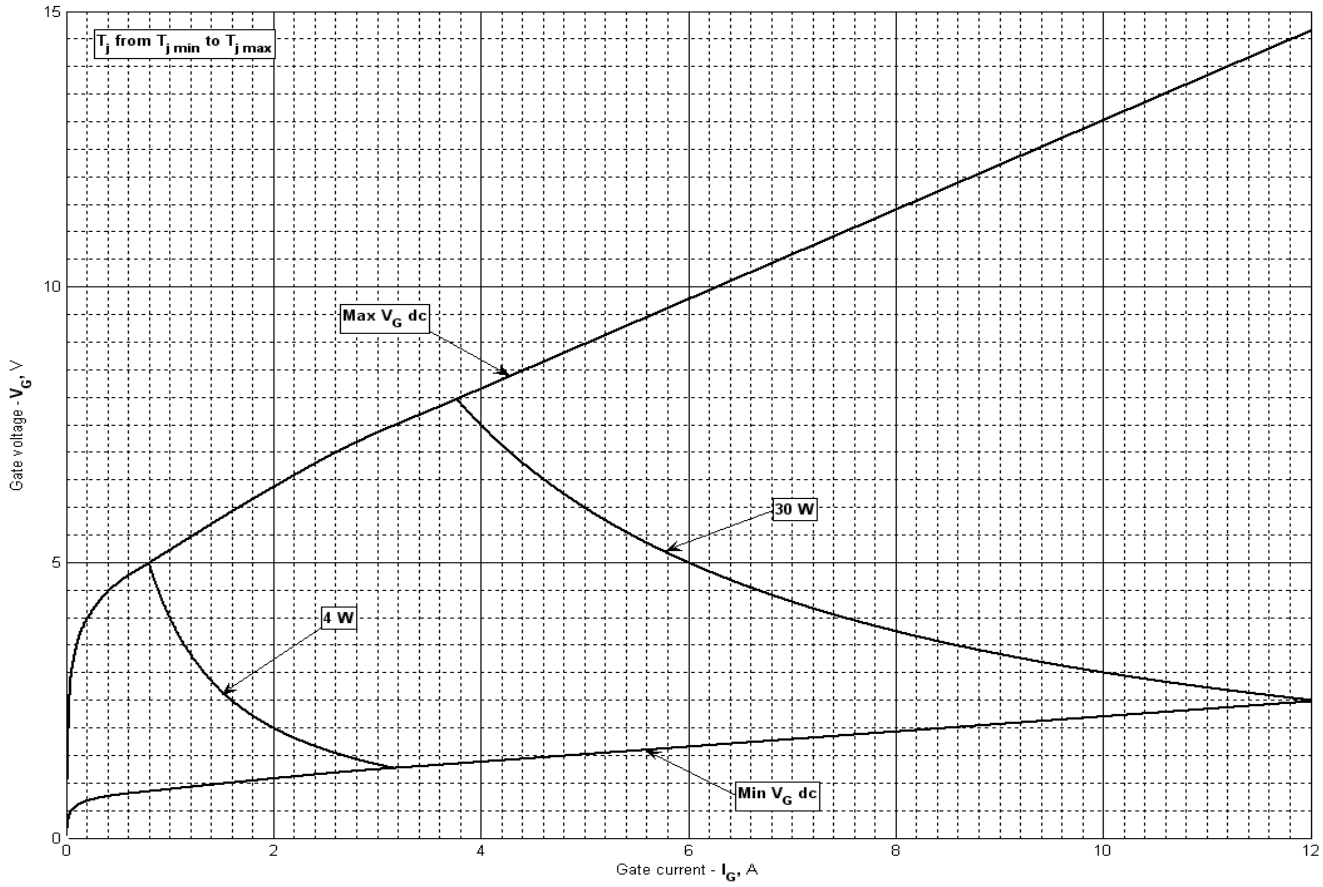


Fig 4 - Gate characteristics – Power curves

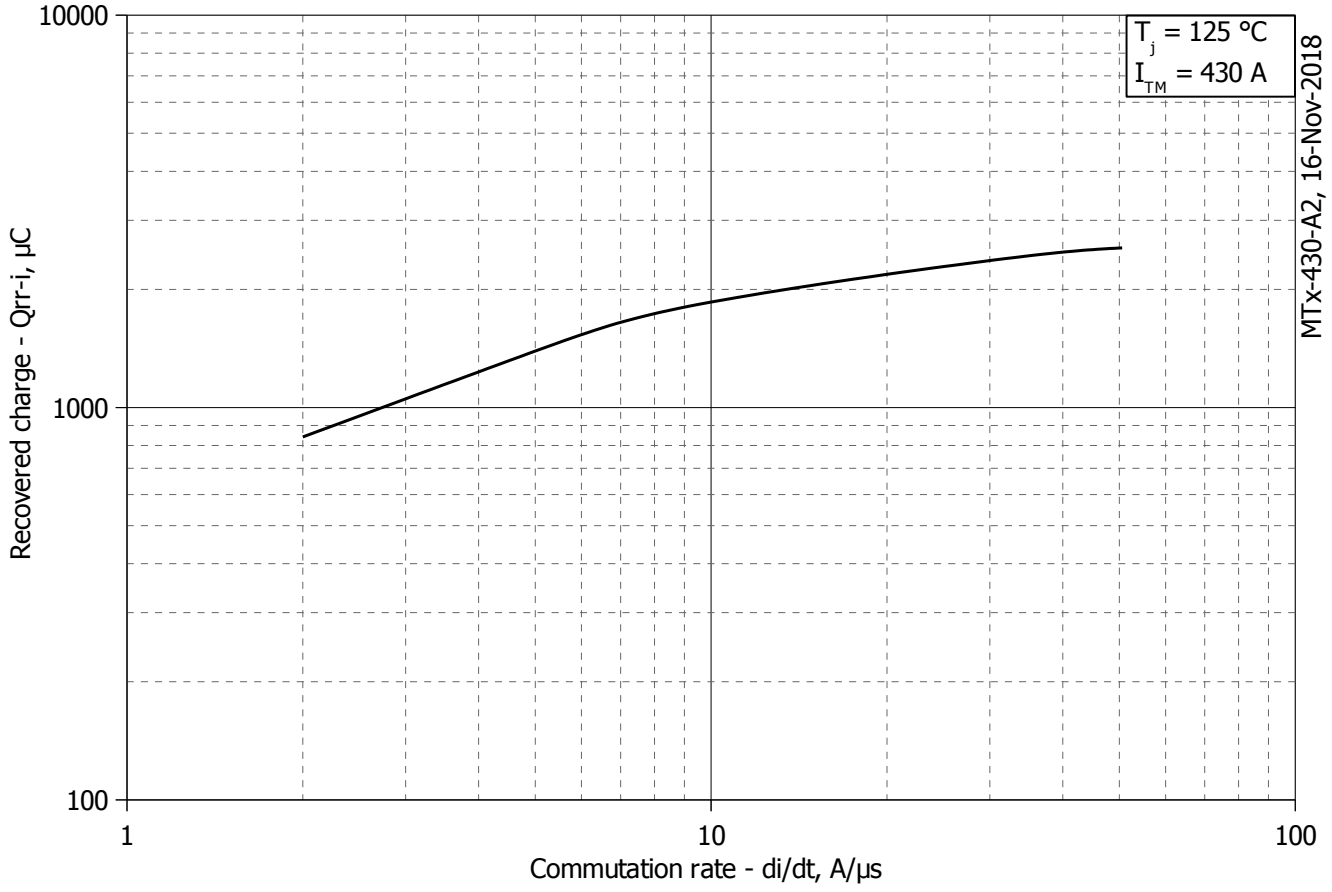


Fig 5 - Total recovered charge, Q_{rr-i} (integral)

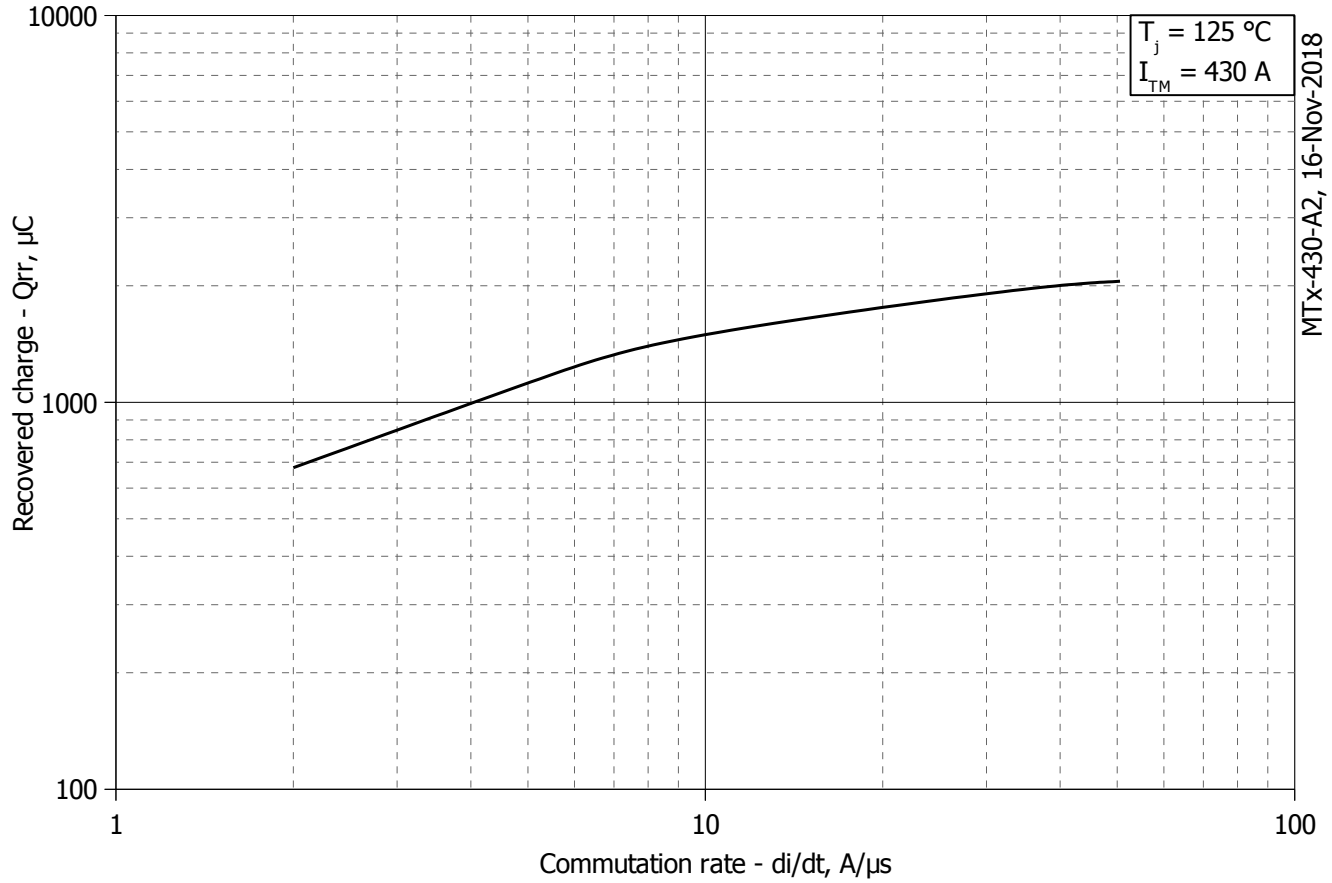


Fig 6 - Recovered charge, Q_{rr} (25% chord)

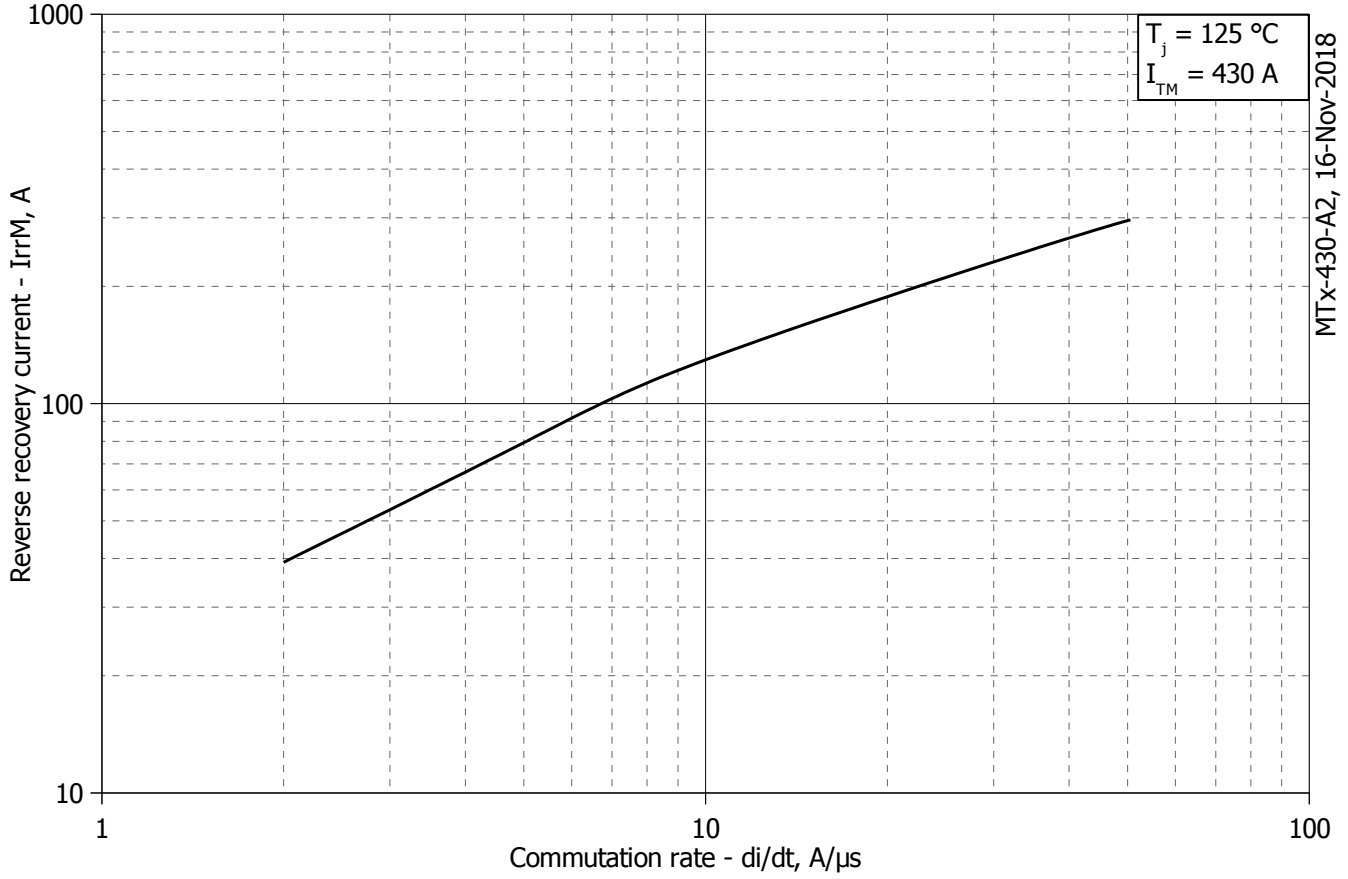


Fig 7 - Peak reverse recovery current, I_{rrM}

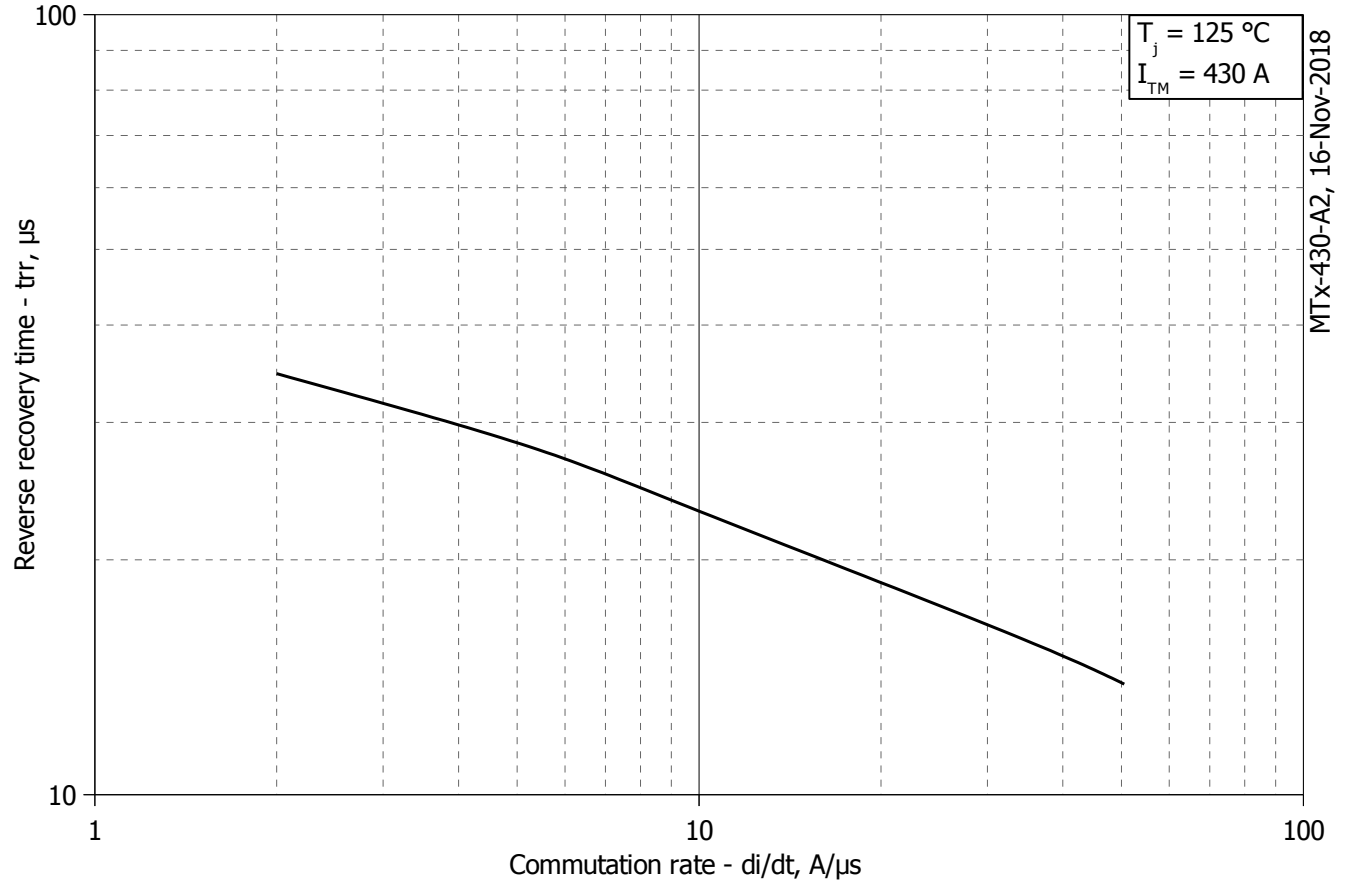


Fig 8 - Maximum recovery time, t_{rr} (25% chord)

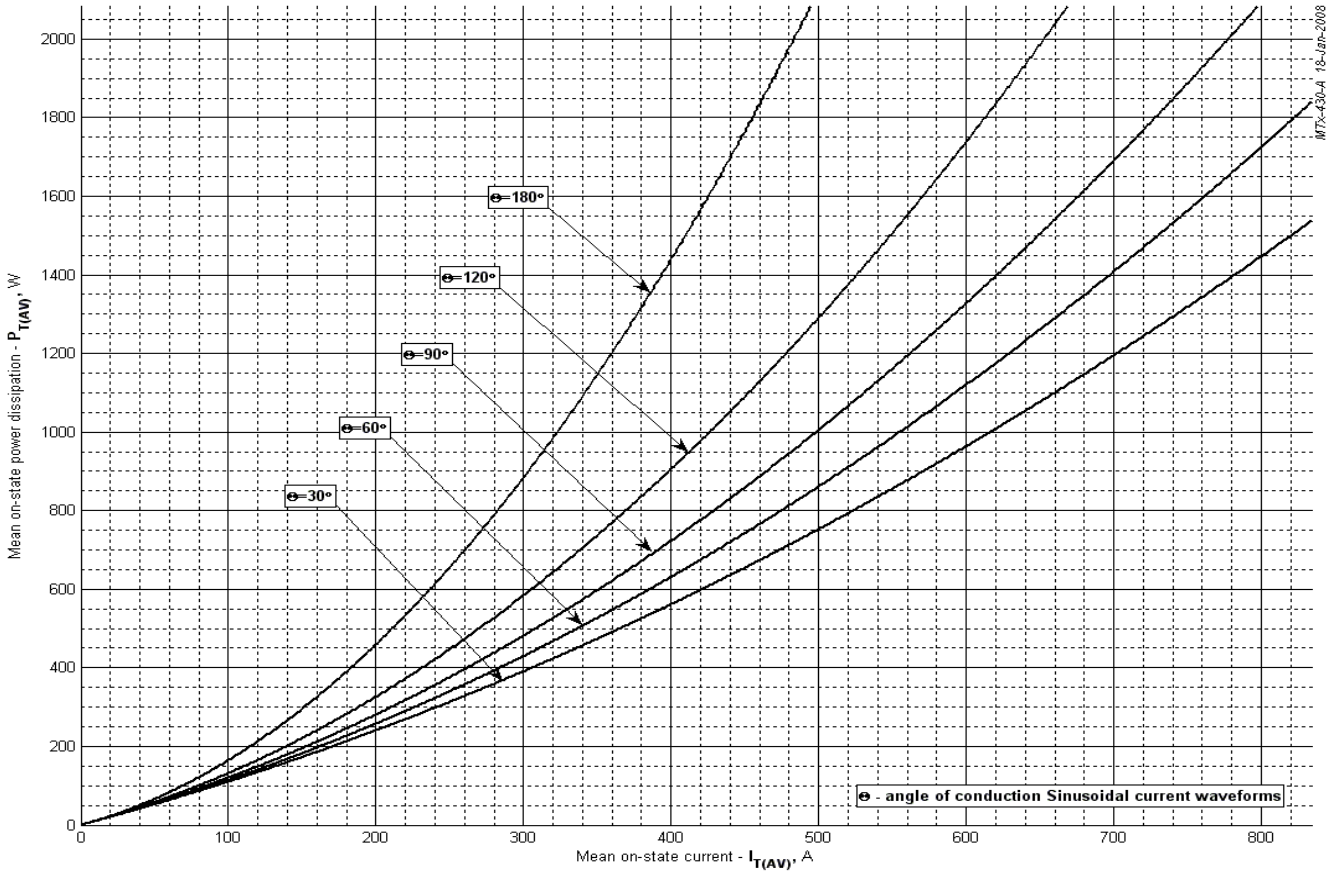


Fig 9 – On-state power loss (sinusoidal current waveforms)

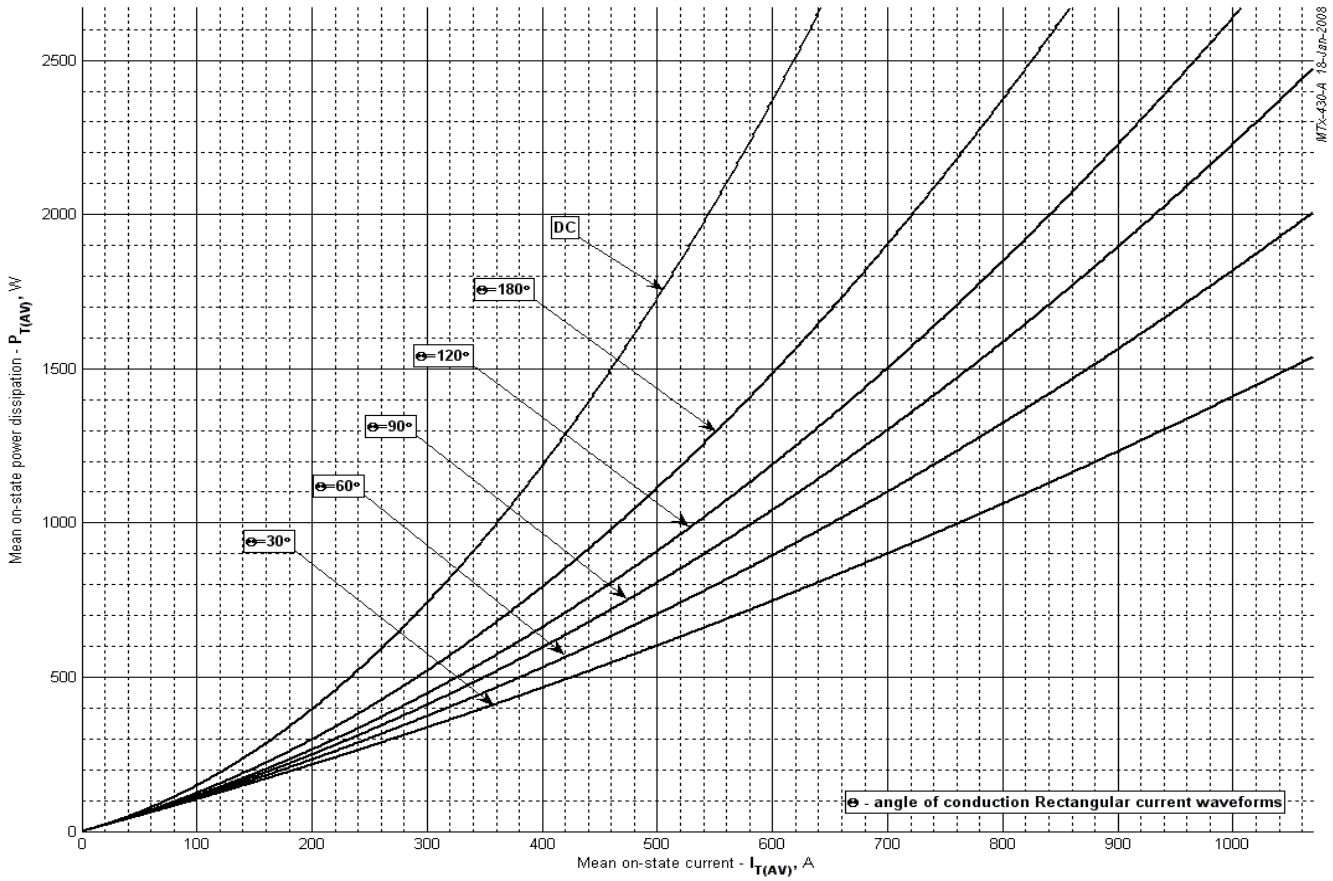


Fig 10 - On-state power loss (rectangular current waveforms)

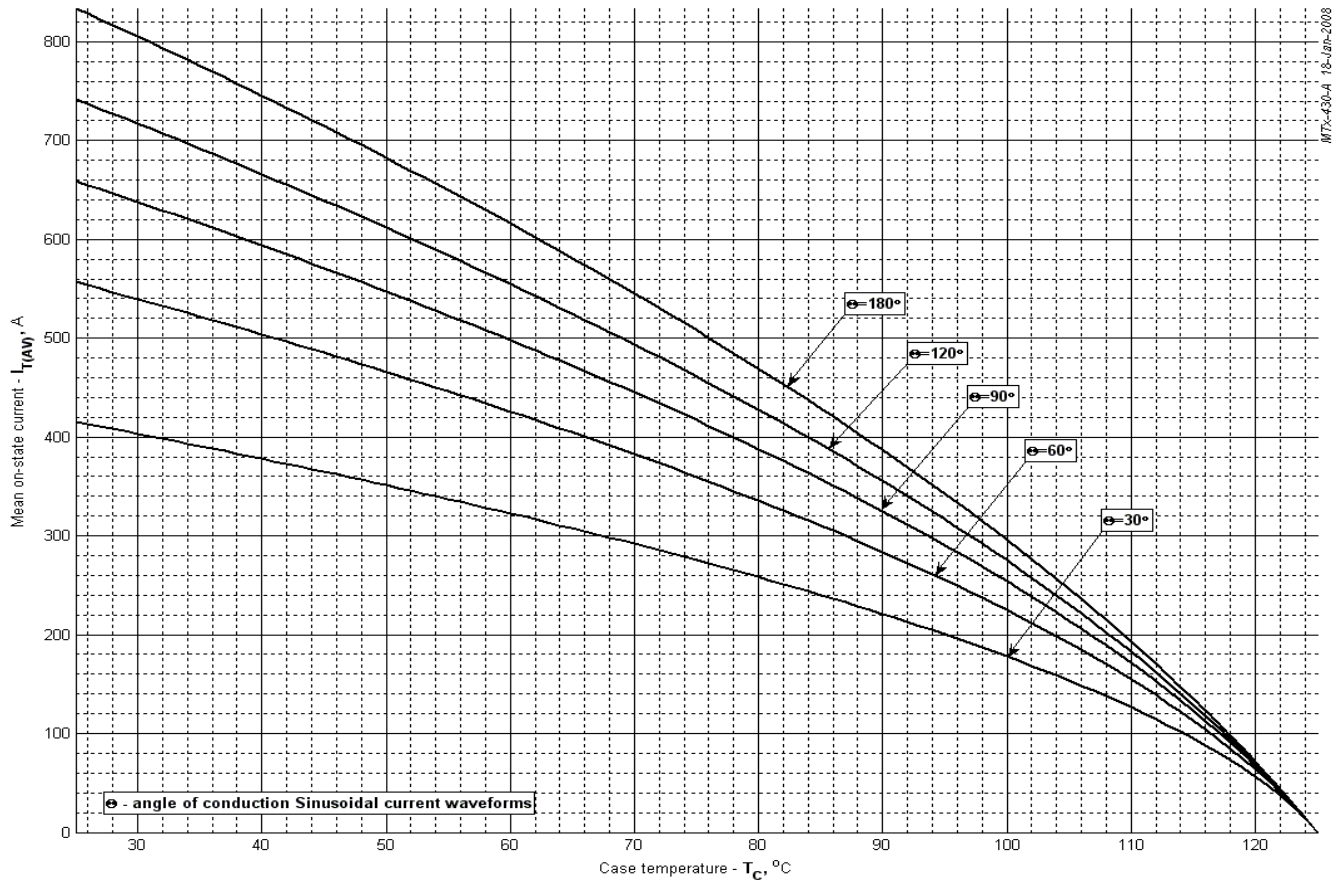


Fig 11 – Maximum case temperature (sinusoidal current waveforms)

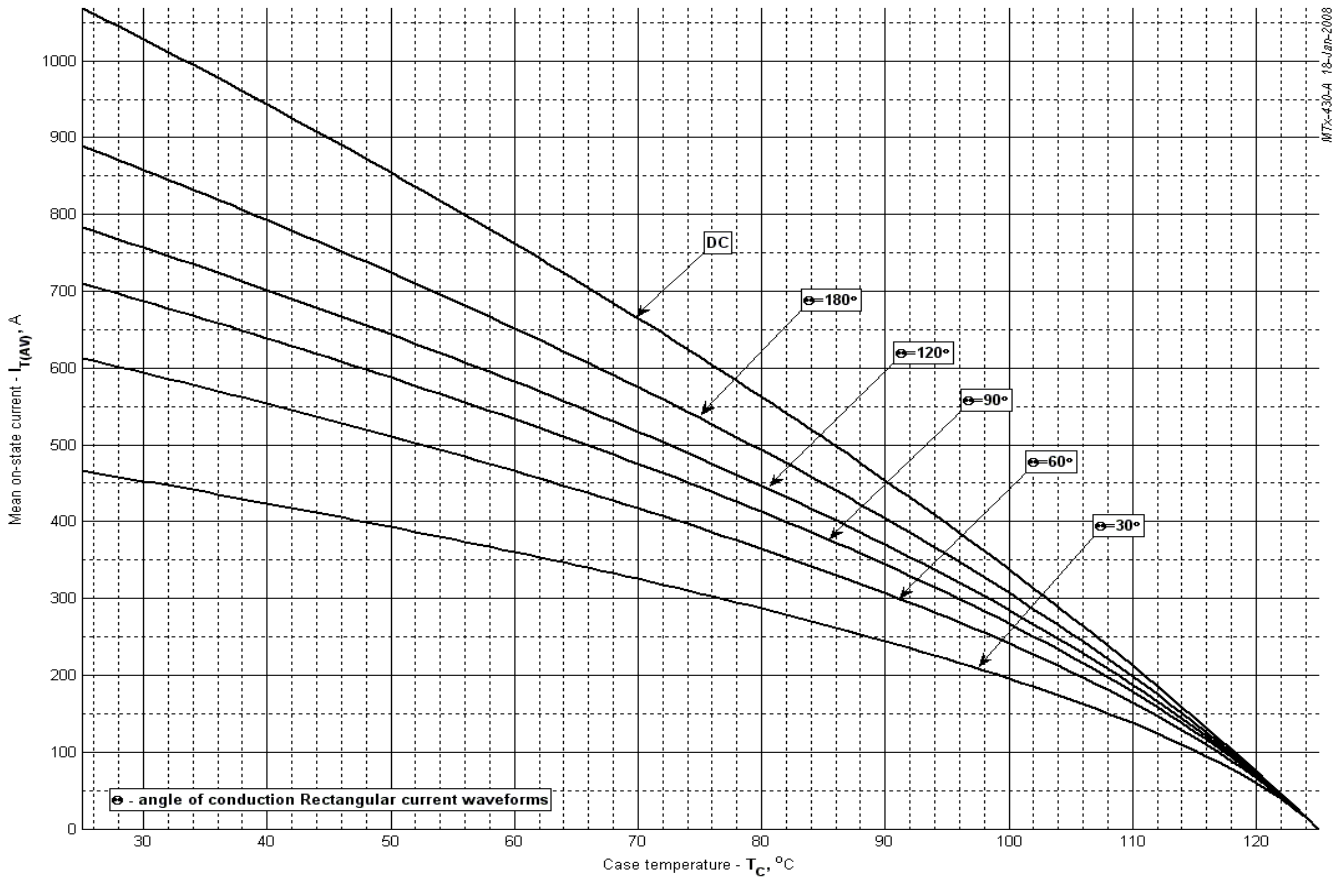


Fig 12 - Maximum case temperature (rectangular current waveforms)

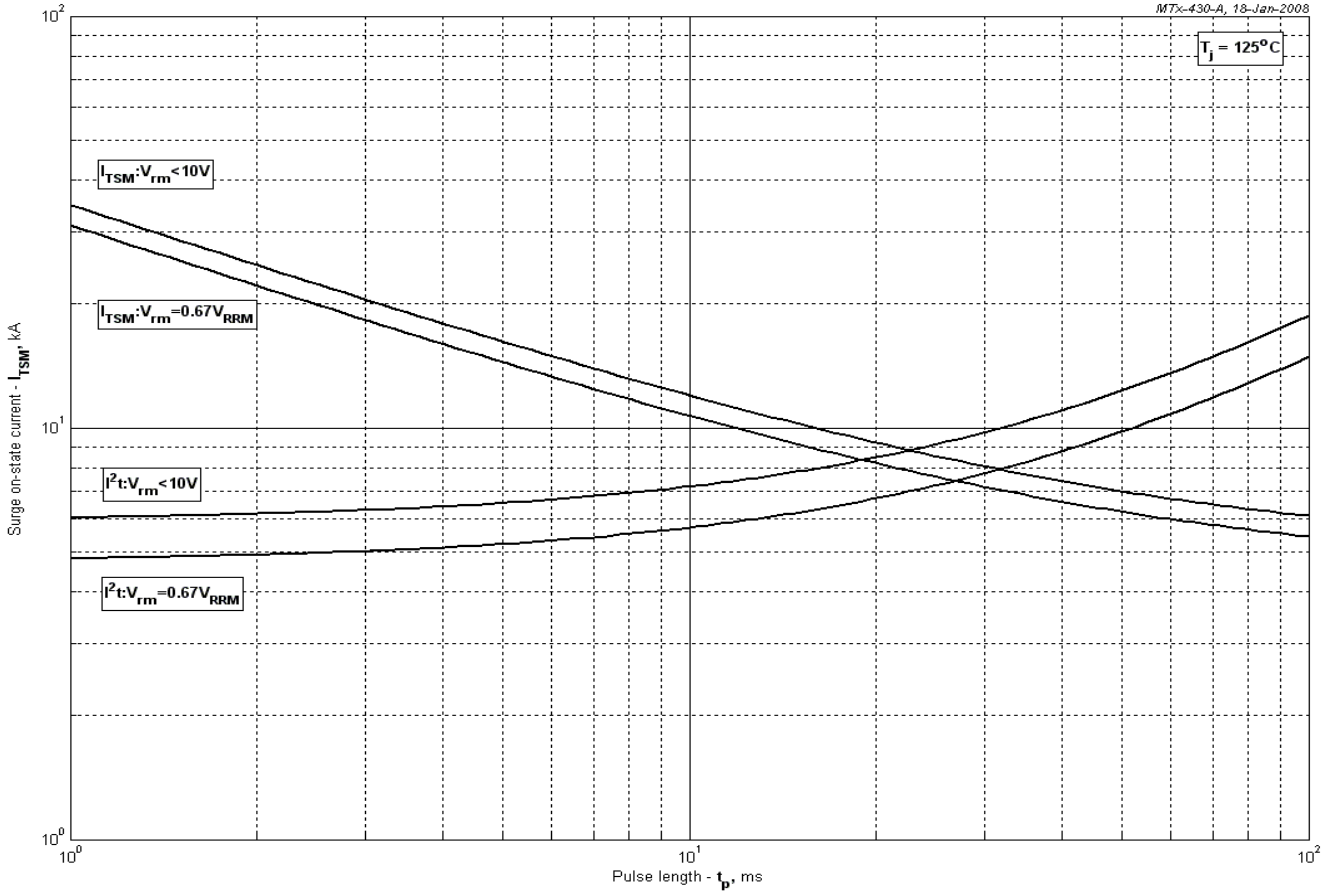


Fig 13 – Maximum surge and I^2t ratings

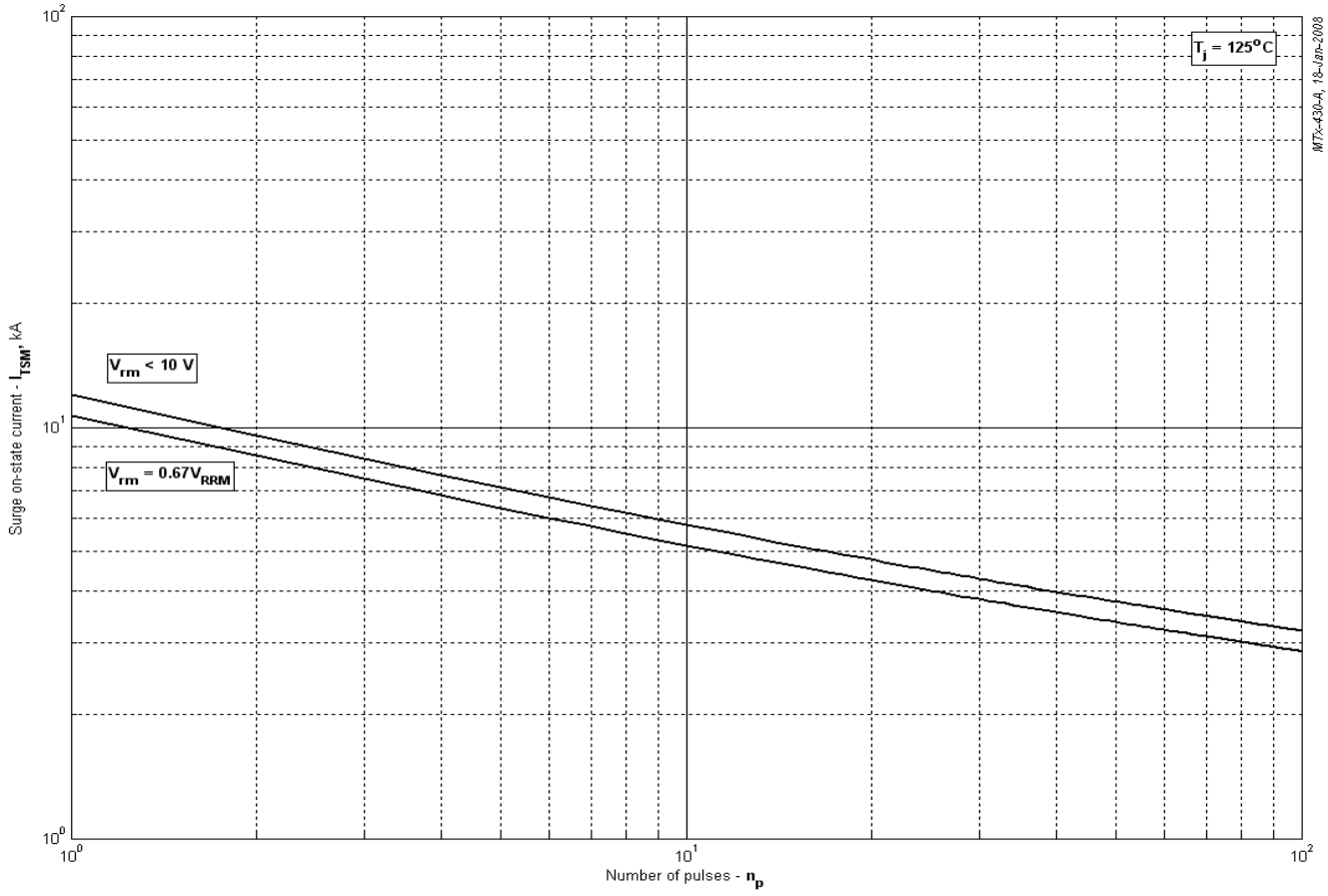


Fig 14 - Maximum surge ratings